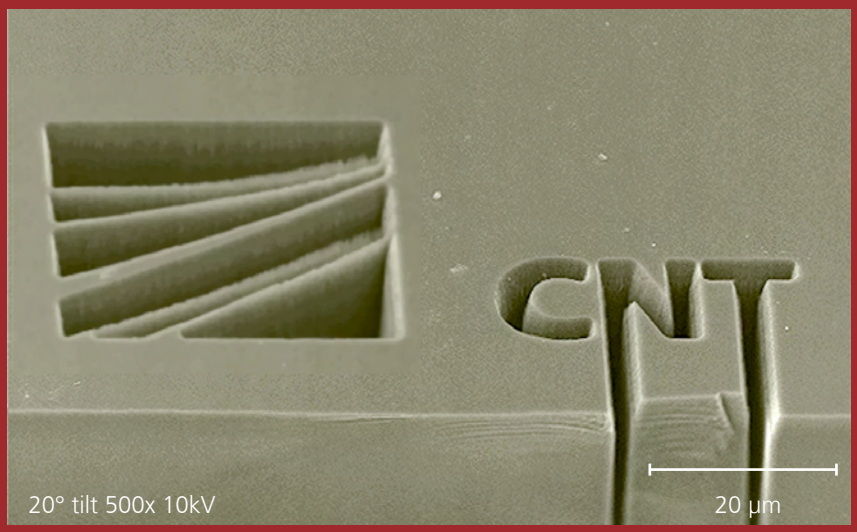
Fraunhofer

CNT

FRAUNHOFER CENTER NANOELECTRONIC TECHNOLOGIES



ANNUAL REPORT 2009

Cover picture

SEM-shot: Preparation of target structure for determination of etch profil within silicon substrat

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The year 2009 has been a turbulent year for our institute. For the microelectronic site Dresden and for Europe it has been a very meaningful year.

Due to the insolvency of our cooperation partner Qimonda we lost an important research partner within Fraunhofer CNT. Generally speaking it means that the only major manufacturer in the field of volatile memory chips in Europe which concentrated its competence in R&D as well as his platform for its worldwide fabrication activities in Dresden does not exist any longer.
Despite intensive efforts of different organizations such as SEMI Europe and an open letter of more than 50 scientists to the Federal Chancellor in addition, it was not possible to succeed in convincing politicians of the relevance of the company for the high-tech site of Germany and Europe. For the future the development of 3-dimensional chip integration is of high importance. Therefore, a memory manufacturer in Europe is necessary.

A further development is related to the structural change of the value chain of the fabrication of logic devices. Foundries which cover a wide rage of products and technology are becoming more and more important. These foundries are able to offer their range more cost-efficient than in-house fabrication even if volumes are changing.

The decision of Advanced Micro Devices (AMD) shows that this also applies for leading-edge technologies with structures beyond 65 nm. AMD and the investor ATIC (Abu Dhabi) have founded a joint venture named GLOBALFOUNDRIES. With the acquisition of Chartered Semiconductor (Singapur) and the set-up of a new manufacturing site in Albany, N.Y. (USA) GLOBALFOUNDRIES will orientate its activities more globally. The partnership with GLOBALFOUNDRIES offers Fraunhofer CNT a wide field of R&D topics which can be executed together with the institutes of Fraunhofer Group of Microelectronics.

Reorientation of Fraunhofer CNT

The changed situation requires an adjustment of Fraunhofer CNT. This process has been started with several strategy workshops and will be proceed continuously.
Within the next years we will continue to work together with GLOBALFOUNDRIES Dresden Module One LLC & Co. KG focusing on the „Leading Edge“ development of structures beyond 35 nm. In parallel we will use our established competencies within the fields of Functional Electronic Materials, Devices & Integration, Analytics as well as Patterning to push forward R&D in „More than Moore”.

Core area of R&D will be the development of technologies for „Leading Edge Nanoelectronic".

In this difficult situation of transformation, caused by the insolvency of Qimonda, the Fraunhofer CNT was essentially supported by the funding organizations of the State of Saxony and of the Federal Ministry of Germany. Thereby we were able to maintain a reliable partner within running projects and continue our cooperation with other research organizations, universities and institutes.

The year 2010 will be essential for our institute especially in view of a solution of the location question which is still open. Currently we are using clean-room, labs and offices from Qimonda. Due to the constructive cooperation with the insolvency administrator it was possible to hold up our operating business. However, a long-term solution is necessary.

With this report we would like to give you an insight into our wide range of research activities. Furthermore, it shows the performance and innovation of our institute.

Dresden, June 2010

Prof. Dr. Peter Kücher

FRAUNHOFER CNT

Research and Development at Fraunhofer CNT

The business area of Fraunhofer CNT include the development of processes and materials as well as the physical and electrical characterization of high-performance-logics, derivates (e.g. embedded DRAM) and memory technologies for volatile and non-volatile devices. In close cooperation to industrial partners and to other R&D organizations the objective of our institute is to develop innovative unit process solutions for nano-electronic systems on 300 mm silicon wafers. The aim is to transfer research results fast into industrial manufacturing.

The service offer of Fraunhofer CNT is devided into four fields of competence: :

- Analytics
- Functional Electronic Materials
- Devices & Integration
- Patterning

Equipment

At present, the Fraunhofer CNT uses 800 m² clean-room area (class 1000) and an infrastructure which meets industry standard. In addition to 40 clean-room tools scientists at Fraunhofer CNT use considerable analytical and metrological processes for R&D as well as for the characterisation of nano-electronic devices. The institute does not maintain a continuous process line to cover all necessary process steps in order to realize high-integrated memory chips. However, Fraunhofer CNT possesses of new process tools which are typically for production on which scientists are able to do research and development with their partners. Sub-processed wafers are being provided from the cooperation partners – innovative proczess steps will be operated at Fraunhofer CNT. That way the delivered results can be transferred into manufacturing immediately. This enables the partners to reduce their capital expenditures. Beyond that a faster time-schedule is possible.

Cooperation partner within direct environment

The Fraunhofer-Center Nanoelectronic Technologies was founded in 2005 according the model of a Public-Private-Partnership. Besides the successful cooperation with the semiconductor manufacturer GLOBALFOUNDRIES Dresden Module One LLC & Co. KG the institute is open for the cooperation and execution of projects with different research organizations, industrial partners, universities as well as semiconductor suppliers such as material and tool manufacturers.

Within direct neighbourhood of Fraunhofer CNT the semiconductor manufacturers GLOBALFOUNDRIES, Infineon and X-Fab are located. In addition, Dresden and Silicon Saxony offer excellent site conditions. Because of the close proximity to the manufacturing lines of the partners and of the established know-how, Fraunhofer CNT benefits of numerous synergy effects. That way it is possible to implement innovative developments and new processes fast into manufacturing. It also enables the partners to save time and production costs.

„Benefiting of synergies between the reference of the manufacturing lines, on the basis of latest 300 mm wafer-technology, as well as of the know-how of our employees, it enables us to perform our projects successfully and immediately."
Prof. Dr. Peter Kücher

Employees at Fraunhofer CNT

FRAUNHOFER CNT IN FIGURES

The Fraunhofer CNT generated in 2009 earnings of about 7.7 Mio. Euro – compared to expenditures with the amount of about 10.8 Mio. Euro. The deficit of revenue in 2009 is a result of the insolvency of our cooperation partner Qimonda. In 2009 the operation budged composes of about 41 % of industry returns, about 18 % earnings out of national public projects, about 14 % of EU-earnings and about 27 % of other output.

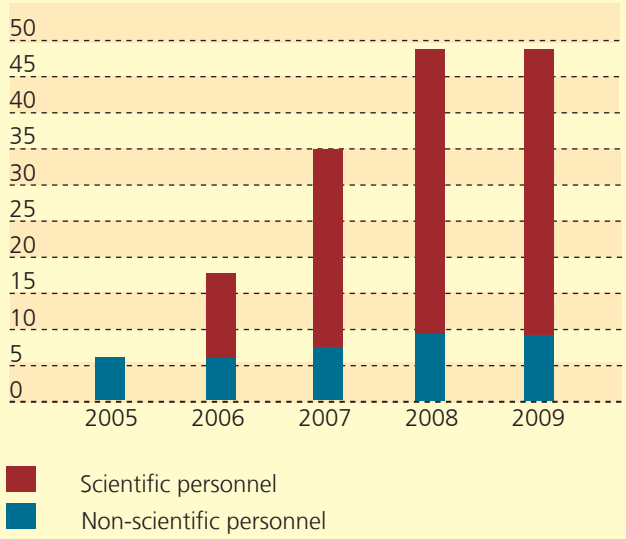
Due to the continuous partnership with GLOBALFOUNDRIES Module One LLC & Co. KG the main investor comes from the industry. Public earnings result especially out of the projects I-COSEL and BRIDGE. Within the Saxon R&D project I-COSEL scientists from Fraunhofer CNT studied together with their colleagues from Fraunhofer ENAS the development of nano-interconnects and MEMS/NEMS via electron beam lithography. The project BRIDGE which is funded by the BMBF focuses on the development of basic technologies in order to implement the ITRS roadmap. The objective of the R&D project BRIDGE is to provide, especially for critical unit processes such as patterning, etching and deposition, innovative solutions for the production of micro chips on the basis of 300 and 200 mm wafers. A further aspect is the integration of unit processes as well as the further development of analytical methods. On the European side the Fraunhofer CNT is involved in two major projects within the 7. Framework-Programme (ICT). The project MAGIC concentrates on the development of mask-less electron beam lithography for the manufacturing of micro chips. Therefore, two different methods of multi-electron beam lithography are being evaluated. With its Center of Competence E-Beam the Fraunhofer CNT inserts its outstanding know-how of mask-less pattering of smallest semiconductors. Topic of the EU-project named GOSSAMER is the further development of a trendsetting trapping based non-volatile memory concept. The aim of the project consortium, which is led by the semiconductor manufacturer Numonyx, is the development of a demonstrator on the basis of sub 40 nm process technologies.

Expenditures and Revenue 2009

	in T €	in %
Annual Budget 2009	**10.820**	
Expenditures	**10.820**	
Personnel Expenses	2.378	22,0
Non-personnel Expenses	8.182	75,6
Allocation (head office)	248	2,3
Invest	12	0,1
Revenue	**7.660,2**	
Industrial Projects	3.127,8	40,9
Public Projects (national)	1.387,8	18,1
Public Projects (EU)	1.090,0	14,2
Others	2.054,6	26,8

Development of Operating Budget 2006 - 2009

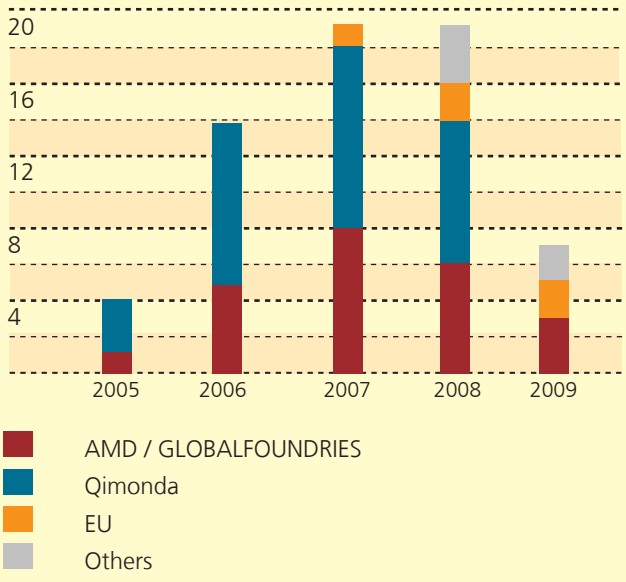
Personnel Development 2005 - 2009



By the end of the year 2009 Fraunhofer CNT employed 49 permanent staff. The personnel structure was put together as follows: 35 scientists including 20 Ph.D. Students, 2 diplomats, 5 technicians and 7 administration personnel.

Equipped with professional project management, latest lab equipment, intense initial research and a long-lasting industry know-how, employees of Fraunhofer CNT provide support to their international customers and partners in order to make innovations useful for the future.

Project Development 2005 - 2009



So as to professionally process R&D assignments Fraunhofer CNT possesses of 800 m² clean-room area and 130 m² laboratory area which are arranged with the latest semiconductor R&D tools. The equipment spans from deposition and etch tools used for the heat treatment at high-temperatures as well as from inspection and analytic tools which are used for the characterization of defects and layers.

INNOVATION TROUGH COOPERATION

FRAUNHOFER GROUP FOR MICROELECTRONICS

VµE Business Areas:

Ambient Assisted Living
Energy Efficient Systems and eMobility
Communication and Entertainment
Light
Security
Technology

The Fraunhofer Group for Microelectronics (VµE) coordinates the activities of the Fraunhofer institutes working in the fields of microelectronics and microintegration.

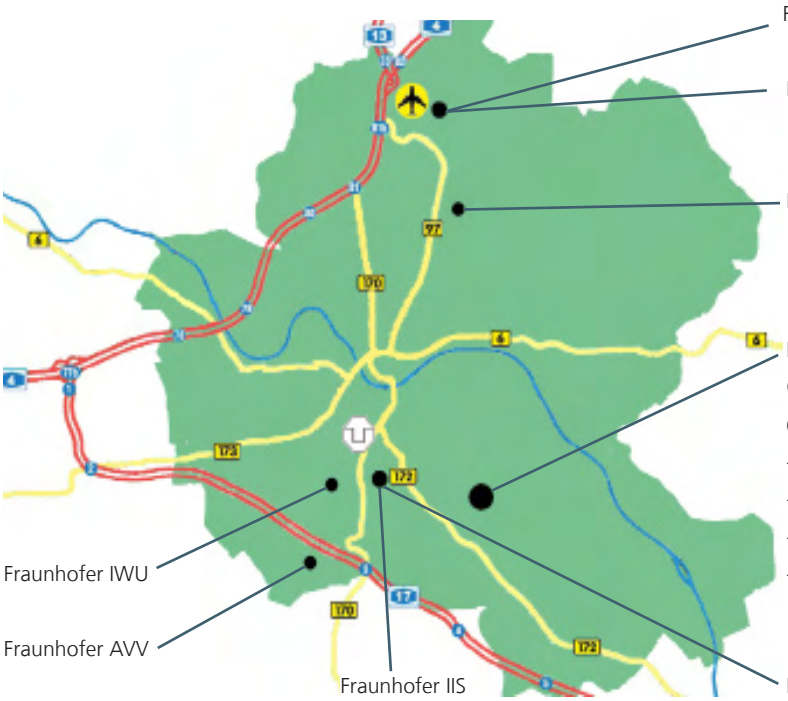
The Fraunhofer CNT is contact for the business area "Technology" which consists of two divisions: »More Moore" and „Beyond CMOS".

The Group's expertise spans from classic CMOS technology to the use of innovative nanotechnologies. Apart from silicon, this also includes compound semiconductors and new materials. Expertise in developing CMOS and other device technologies for microelectronics forms the basis for both technological services and application-specific component development.

FRAUNHOFER IN DRESDEN: CLUSTERED RESEARCH

The Fraunhofer Gesellschaft is represented in Dresden by six institutes and six other facilities. The twelve Fraunhofer facilities together employ more than 1,100 employees with an annual turnover of more than 100 million Euros.

In addition to the extraordinarily high density of research facilities, the region is characterized by the close interlinking of research and industry, resulting in the creation of new first-class services and innovative developments, which then go on to make a global impact.



REVIEW OF FRAUNHOFER CNT RESEARCH: RESULTS/APPLICATIONS

The key activities of Fraunhofer CNT focus the development of innovative processes for high-performance-transistors as well as of nanoelectronic integrated circuits. The service offer of Fraunhofer CNT is devided into four fields of competence.

Analytics

Functional Electronic Materials

Devices & Integration

Pattering

ANALYTICS

COMPETENCE AREA ANALYTICS

Characterisation of materials

The competence area Analytics concentrates on the characterization of materials, needed for the fabrication of modern semiconductor chips. It focusses on topics such as the distribution and activity of dopants, properties of surfaces und interfaces, crystallization and phase formation, lateral resolved stress measurements and quantification of impurities. In order to meet the challenges of ongoing miniaturization, we engage in the improvement of existing methods and also in the application of new methods, e.g. atom probe tomography.

Competence
Analytics

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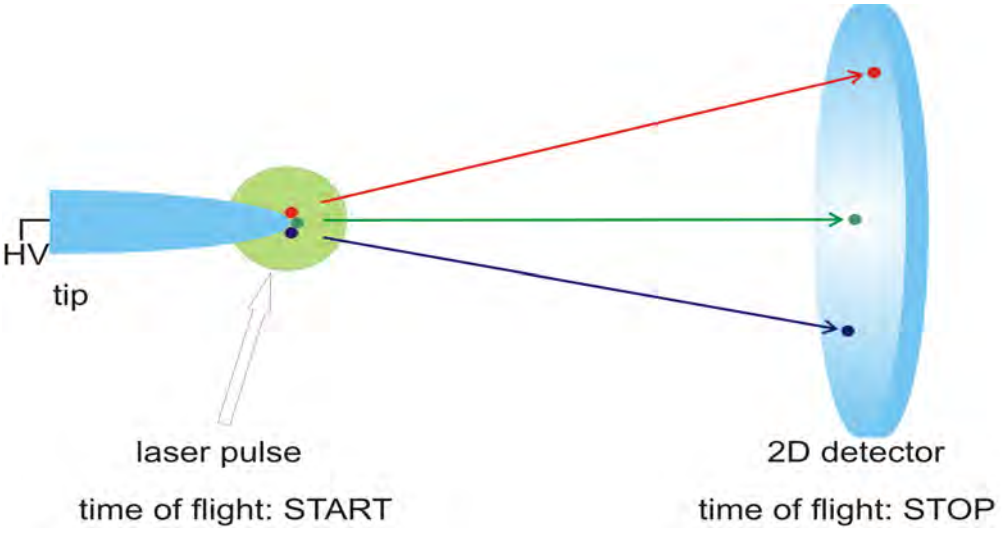
Dr. Lutz Wilde
Group leader
Analytics

ANALYTICS

Material analysis via Atom Probe Tomography

The continued scaling of high performance CMOS devices has been accompanied by the introduction of an increasing number of new materials. Examples include the replacement of SiO2 based gate dielectrics by HfO2 based high-k dielectrics and the replacement of poly-Silicon based gate electrodes by metal gate electrodes. As the gate dielectric has a thickness of only a few nanometers, the development of processes for the manufacturing of such layers has created a demand for analytical techniques that permit quantitative compositional 3D imaging with sub-nm spatial resolution. One candidate for achieving this goal is Atom Probe Tomography (APT), the principle of which is depicted in fig. 1. In APT, a Focused Ion Beam (FIB) is used to shape the material to be analyzed into the form of a tip with a spherical end cap of less than 100 nm radius.

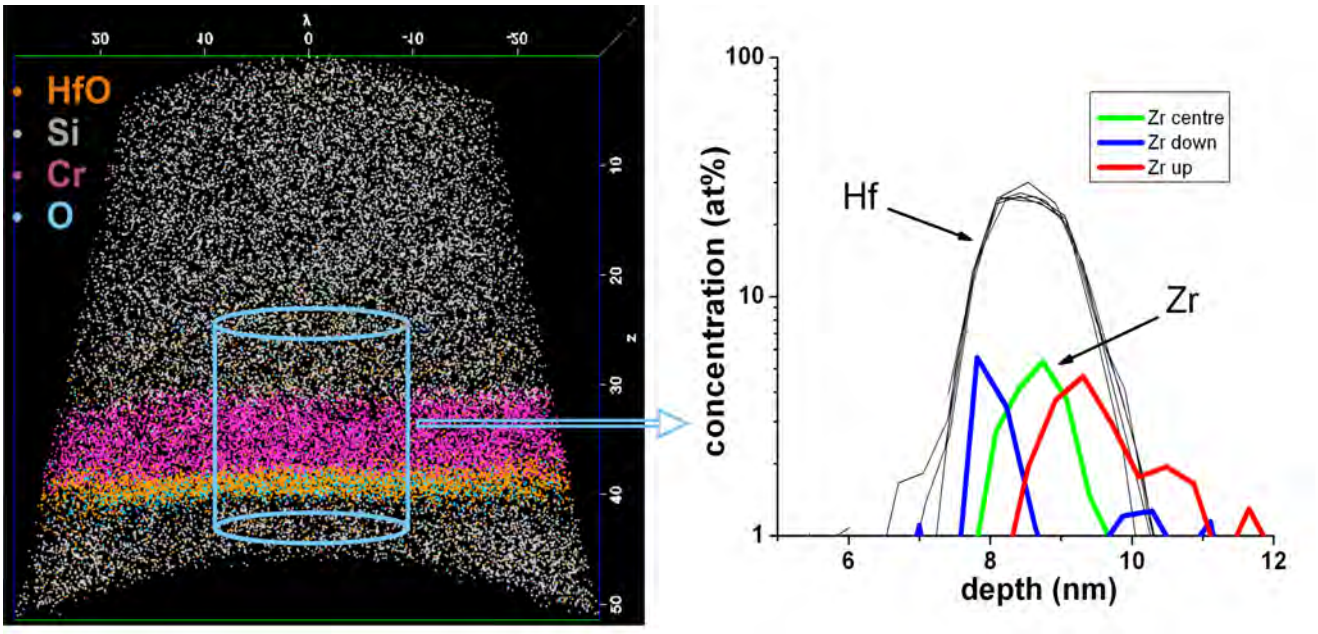
When a sufficiently high voltage is applied to this tip, the atoms at the tip surface are field ionized and accelerated towards a 2-dimensional position-sensitive detector, a process known as field evaporation. This setup constitutes an ion-optical point projection configuration, in which the tip surface is imaged onto the detector. The moment of field evaporation can be triggered by applying laser pulses to the tip, thereby permitting to both control the evaporation process and to determine the flight times, and hence the masses of the evaporated atoms. Since the atoms are field evaporated sequentially, the position of the atoms before evaporation can be reconstructed mathematically to provide a 3D atom map of the sample.



1 *Basic principle of APT operation: At high applied voltage surface atoms are field ionized by pulsed laser and are accelerated towards a position-sensitive detector. The mass of each atom is determined by measured time of flight.*
image source: GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG

In the following we show examples that illustrate the spatial resolution and reproducibility of APT and demonstrate its potential to provide standard-free quantitative results and study the formation of atom clusters. The examples are chosen so as to illustrate in what way APT can be used for the development of processes related to the manufacturing of high performance CMOS transistors.

The first example shows depth profiles and a typical atom map of three samples that were measured in order to evaluate the depth resolution that can be obtained by APT. To this end three HfO2 based dielectrics were analyzed that had a ZrO2 monolayer embedded in a specific depth of the HfO2 layer. The samples were deposited with Atomic Layer Deposition (ALD) in order to control the depth of the ZrO2 layers, which were located at the upper interface, the centre, and the lower interface of the HfO2 layer, respectively. Fig. 2 shows the resulting depth profiles that were extracted from the 3-dimensional atom map. The difference of the position of the ZrO2 layer is clearly confirmed proving that a depth resolution of better than 1 nm



2 *3-dimensional atom map of a high-k layer. Cr and Si act as a protection layer during sample preparation. 3 samples were measured in a similar way and their depth profiles, which were extracted from a similar cylinder shown, are overlayed to demonstrate the sub-nm depth resolution.*
image source: GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG

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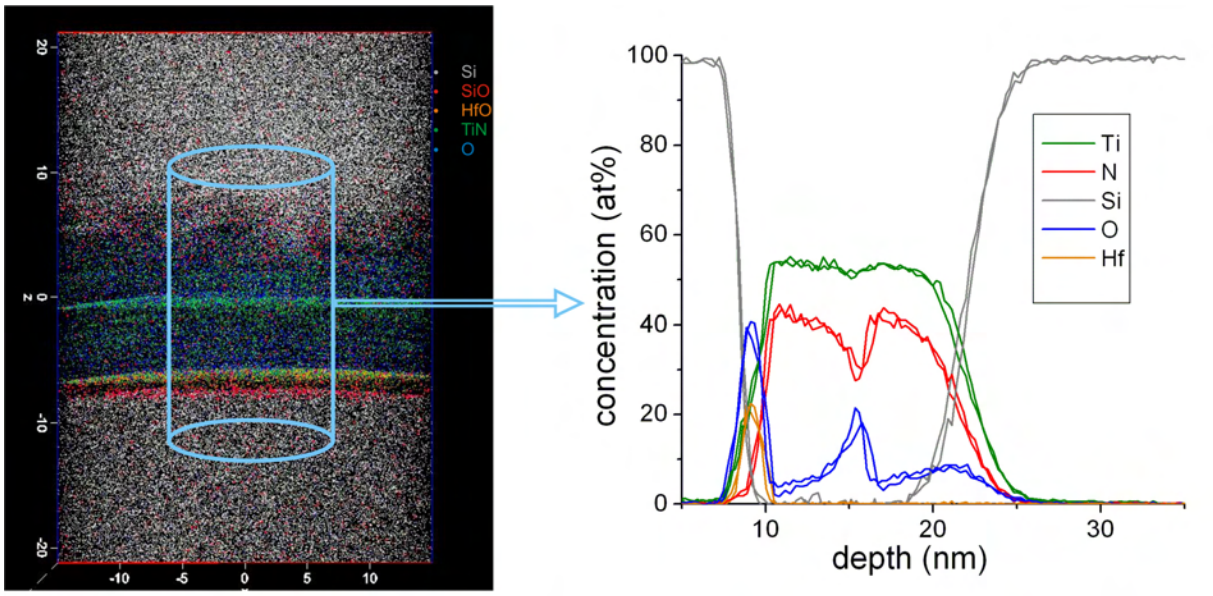
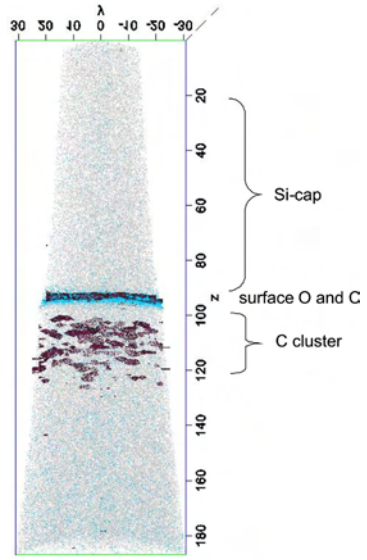
As a second example a high-k/metal gate stack was measured to illustrate both the reproducibility of APT and its potential to provide standard-free quantitative results. An APT atom map of this sample is shown in fig. 3. Excellent reproducibility was observed as exemplified by the overlaid depth profiles of two measurements. At the same time the elemental concentration turns out to be close to the expected stoichiometric composition. Note that the correct quantification was obtained just by counting the atoms in the analyzed volume without referring to standards.



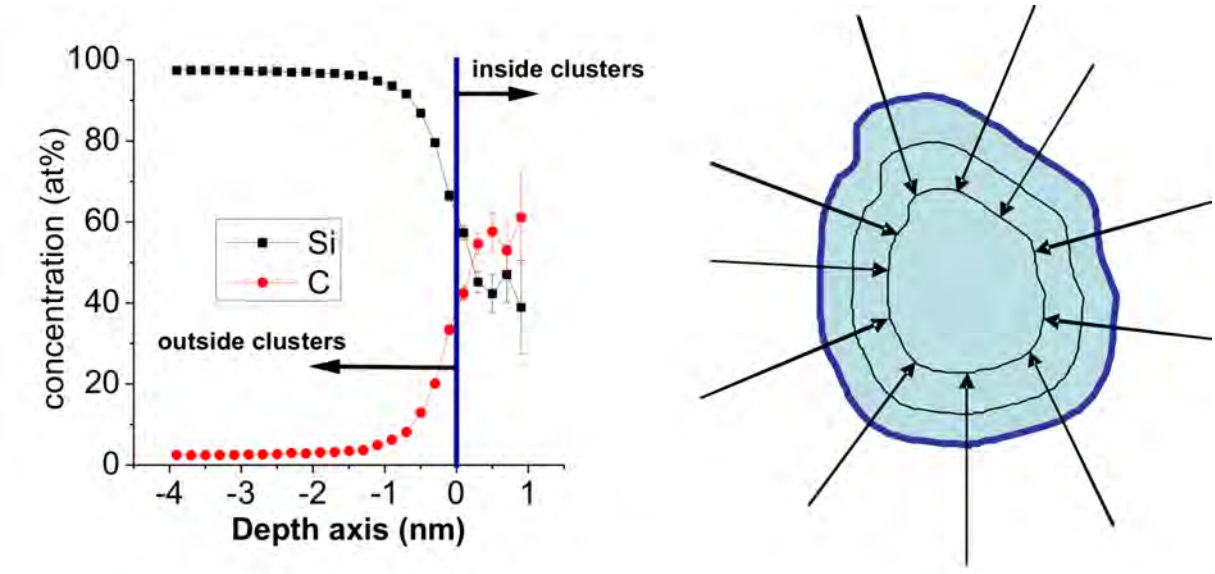
3 *3-dimensional atom map of a high-k / metalgate layer. From a cylinder depth profiles of two measurements of the same material stack were extracted and are overlayed to demonstrate the excellent reproducibility. image source: GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG*

Apart from the extraction of depth profiles 3D atom maps provide the possibility to analyze phase formation and atom clustering. This is illustrated in the third example which shows a Si sample that was subjected to a C implant followed by an anneal. As a result of this procedure C clusters were formed inside the Si matrix, as shown in fig. 4. The visualization of atom clusters is obtained by drawing a surface connecting all points with identical concentration, so called iso-concentration surfaces. In this example the overall C concentration in the implanted volume was 2 at% while the iso-concentration surfaces were drawn at a C concentration of 10 at%. A further analysis of the C clusters can be done by calculating a depth profile relative to the iso-concentration surfaces, going from the outside to the inside of a representative cluster, as shown in fig. 5. This result suggests that a SiC phase formation has taken place.

(Sergej Mutas in cooperation with Dr. Christoph Klein, GLOBALFOUNDRIES)



4 *3-dimensional atom map of a Si sample, which was implanted with C and then annealed. C clusters have been displayed by iso-concentration surfaces.*
image source: GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG



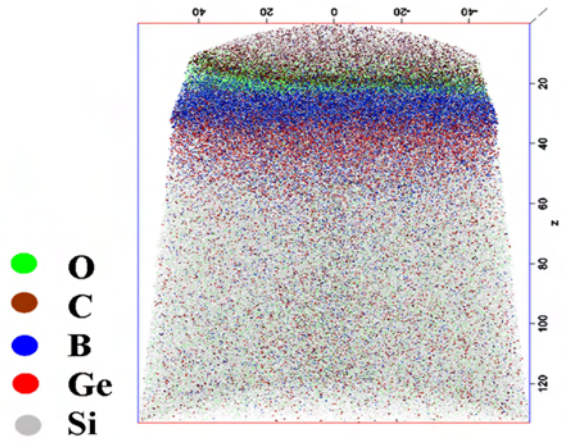
5 *Depth profile of a representative C cluster from fig. 5 relative to an iso-concentration surface from the outside to inside. Phase formation of SiC inside of a cluster can be observed.*
image source: GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG

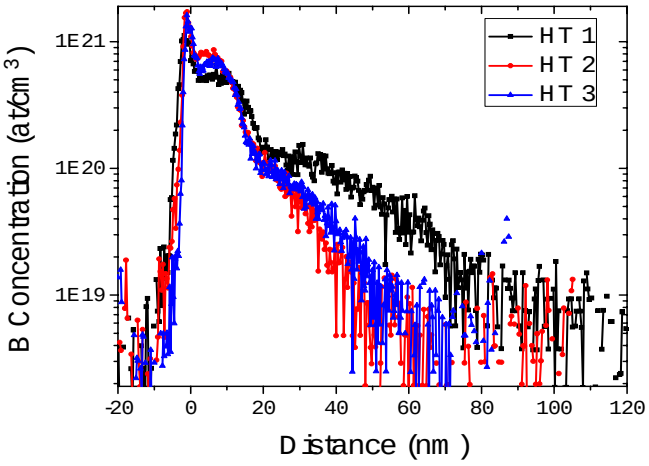
ANALYTICS

Dopant Profiling

Quantitative and qualitative characterization of impurity distribution has acquired increased attention from the semiconductor industry as device requirements have led to high concentration shallow dopant profiles. APT can be utilized for a three dimensional atom mapping of dopant distribution for ultra shallow implants. Distribution of co-implanted B and Ge in Si substrate is shown in Fig. 1.

A quantitative comparison of concentration depth profiles of boron after different annealing temperatures is shown in Fig. 2. Due to different heat treatments; boron has also redistributed differently over depth. Though these differences are small, Hall measurements have shown significant differences in carrier mobility.





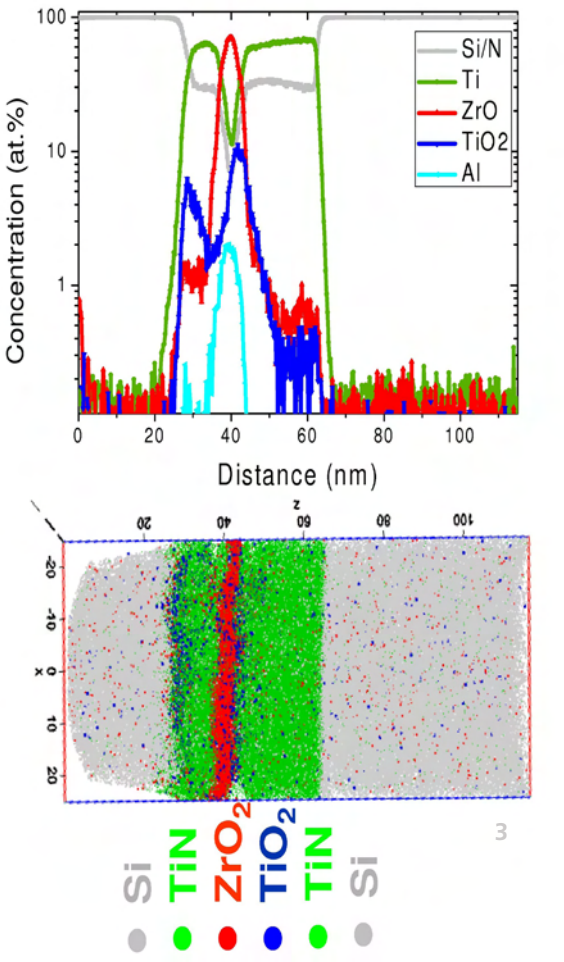
1 *A 2-D atom map showing B and Ge dopant distribution over depth.*

2 *A comparison of concentration depth profiles of boron doped Si, showing small differences for different heat treatment conditions.*

Metal Insulator Metal capacitors

HfO2 or ZrO2 based high k dielectric materials embedded in titanium nitride has been demonstrated as metal-insulator-metal (MIM) capacitors for DRAM and RF applications exhibiting excellent capacitance. Dielectric oxide thickness of 5-10 nm has been used to achieve high capacitances with required leakage currents.

Characteristics of metal-insulator interfaces are of prime interest for the design engineers during different process steps that governs the electrical properties of the resultant products. APT study of such an MIM stack shows a very thin TiO2 layer between (Al-doped) ZrO2 and bottom electrode (see Fig. 3).
A TiO2 seed layer is formed due to the direct exposure of the bottom electrode (TiN) to the ozone during ZrO2 deposition process using ALD. This TiO2 layer is quite difficult to conceive from TEM micrographs. A further investigation of the identical layer stack after high temperature annealing shows out diffusion of ZrO2 and TiO2 on the grain boundaries of bottom electrode as demonstrated in Fig. 4.



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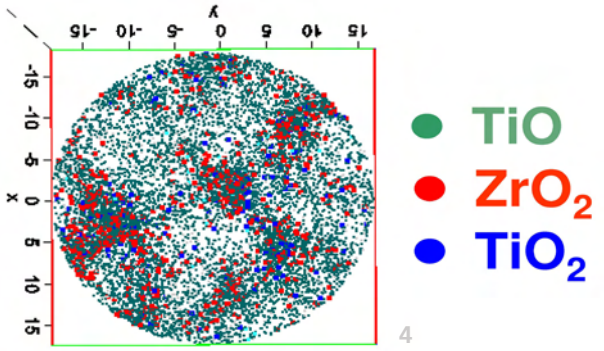

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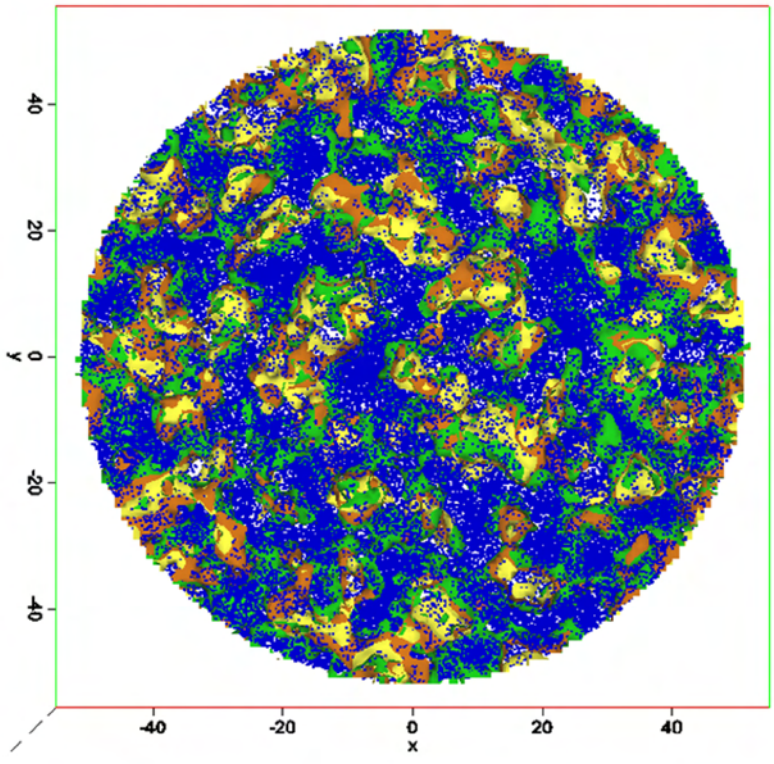
3 A 2-D atom map of the MIM stack analyzed using APT analysis. A concentration profile clearly shows a TiO2 seed layer between insulator and bottom electrode (TiN from the right).

4 A top down view through a 3 nm slice; selected underneath the insulator in the bottom electrode for a MIM stack annealed at a higher temperature (Only selected elements are displayed here for a better visualization). ZrO2 and TiO2 have accumulated on the grain boundaries in the bottom electrode after annealing.

ANALYTICS

A top down view through a 3 nm slice; selected underneath the insulator in the bottom electrode for a MIM stack annealed at a higher temperature (Only selected elements are displayed here for a better visualization). ZrO2 and TiO2 have accumulated on the grain boundaries in the bottom electrode after annealing.
Phase separation within the amorphous state is a possible way to prepare composite metallic glasses which offer excellent mechanical properties. A qualitative and quantitative analysis of phase separation in rapidly quenched amorphous ternary Ni–Nb–Y alloy was done using APT. Thin ribbon (3 mm in width and 30 µm in thickness) of nominal compositions Ni66Nb17Y17 (at.%) were prepared by means of rapid quenching from the melt at a temperature of 1923 K using single-roller melt spinning under argon atmosphere. The spatial distribution of different elements is demonstrated in Fig. 5. Y enriched and Nb depleted (and vice versa) phases are evident with fluctuations from 5-12 nm.
(Dr. Ahmed Shariq)



5 *A top down view through a 2 nm slice; Y enriched phase is shown by regions of blue dots representing Y atoms. 18 at. % Nb iso-concentration surface (light brown), 70 at. % Ni iso-concentration surface (green) and 8 at. % Y iso-concentration (yellow) represent Nb enriched phase.*

Characterization of $Al_{1-x}Si_xO_y$ thin films with ToF-SIMS

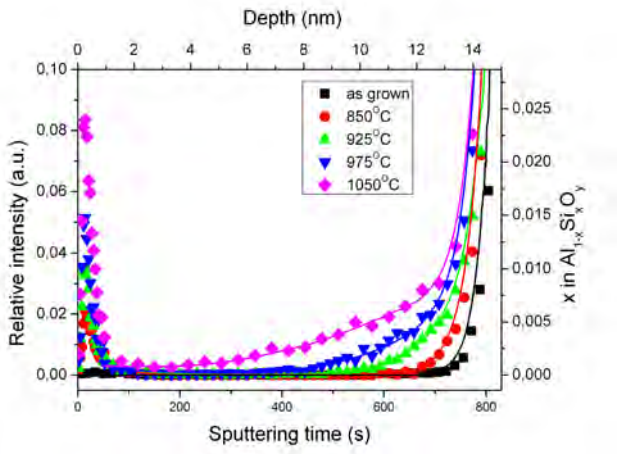
The diffusion of Si from the substrate through the $Al_{1-x}Si_xO_y$ thin films was studied mainly by means of ToF-SIMS. Samples with differences with respect to::

- stack composition: alumina deposited on Si wafer with native oxide or with additional Si_3N_4 intermediate layer
- annealing temperature: from 650 up to 1100°C. Samples crystallizes at around 850°C.
- annealing ambiences: oxygen, hydrogen and nitrogen

The diffusion mechanism was determined and found to be vacancy and grain boundary mechanism for amorphous and crystalline samples, respectively. This was proved by analysis of ToF-SIMS depth profiles on samples annealed with different annealing tem-peratures and ambiences and additionally proved with other analytical techniques like TEM and XPS. The diffusion conditions were not trivial since i) the size of the system was comparable to the diffusion length and ii) Si segregation on top of the layer occurred. Therefore, a source-sink model was proposed with the assumption that every Si atom that diffused to the surface is collected and has no further influence on the diffusion profile, which showed to be a suitable assumption. Fig. 1 presents some of the diffusion profiles with both experimental (symbols) and theoretical (lines) values. The accuracy between experimental data and the simulation was very high. As a next step the diffusion coeffi-cient and activation energy was calculated. It was found to be relatively small (0.88±0.03 eV and 2.29±0.02 eV for amorphous and crystalline samples, respectively) and therefore it was concluded that a large quantity of silicon may diffuse during annealing.

This result was compared with crystalline samples deposited on Si_3N_4 intermediate layer and the activation energy was much higher (3.58±0.02 eV). Additionally it was noted that SiO_2 had a strong tendency to react with $Al_{1-x}Si_xO_y$ forming a rough interface layer. This effect depended strongly on annealing time and Si concentration in alumina thin films and to some extent on annealing temperature. Formation of an interface was not observed for samples deposited on Si_3N_4 intermediate layer. As the last step the surface mobility of Si was determined. The surface diffusion coefficient was found to be two orders of mag-nitude higher than for bulk diffusion and therefore Si did not create islands (typical for grain boundary diffusion) but spread on the whole surface as it was observed by AFM and TEM. All measurements were reproducible and each type of sample was measured at least ten times.

(Paweł Piotr Michałowski)



1 *Diffusion profiles of Si in Al_2O_3 depending on annealing temperature (symbols: experimental data, lines: theoretical calculation)*

ANALYTICS

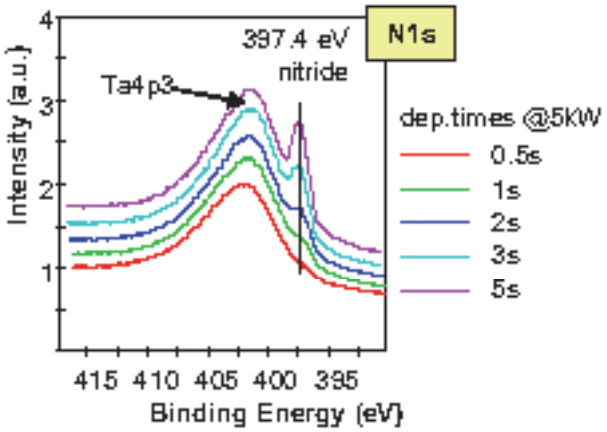
In-situ ARXPS of Thin Barrier Layers

Tantalum/tantalum nitride double layer are used in the semiconductor industry as diffusion barriers between the copper wiring and the surrounding ultra-low-k dielectric in the "back-end-of-line" (Beol). Thereby the quality of the barriers is jointly responsible for the performance of the whole wiring system.

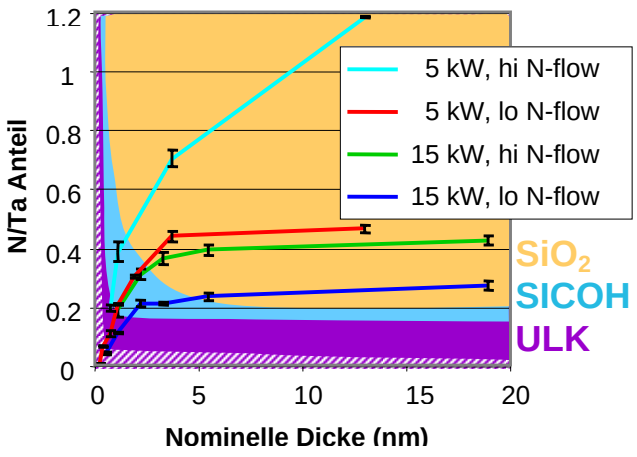
The deposition of the diffusion barrier occurs in two stages, whereas at first a thin tantalum nitride layer (TaN) will be deposited on a dielectric (an organo-silicate glass: dense or porous SiCOH) and then pure tantalum (Ta). Here, the influence of various parameters of the deposition on the quality of the TaN layer, as power, nitrogen flux and deposition duration, are studied. Tantalum based layers are very sensitive to oxidation and thus are losing their desired properties when exposed to atmospheric oxygen. Therefore, for the study of the quality of the barrier layers in-situ measurement methods are inevitable.

X-ray photoelectron spectroscopy (XPS) allows the surface sensitive characterization of layers in respect to their quantitative chemical composition and their chemical binding states. Through angle resolved XPS (ARXPS) it is also possible to determine the layer sequences and thicknesses up to about 5 nm. In the Fraunhofer CNT therefore an ARXPS chamber was attached to a commercial available deposition cluster tool for 300 mm wafers, where the wafers can be investigated directly after tantalum deposition without breaking the ultra-high vacuum.

The reaction of TaN with the dielectric has been studied as function of deposition time. Thereby it was found that initially tantalum oxide, silicide and carbide species formed at the interface. The nitrogen content in TaN increases as a function of deposition time (fig. 1).



1 *XPS- nitride signal at different deposition times.*



2 *α-tantalum growth for different TaN-deposition parameter. Shown for SiO_2 with the additional area gain for the deposition on SiCOH and ULK. Hatched area shows mixed phase growth.*

By means of quantitative XPS depth profiling the layer sequence and layer thicknesses can be reconstructed. Particularly nitrogen-rich TaN layers can be generated by reducing the deposition power and increasing the nitrogen flow. However, these layers have a lower growth rate. For sufficiently thick layers nitrogen saturation will be formed in the tantalum nitride, in which the N/Ta ratio is a function of the combination of both parameters (fig. 2). The subsequent deposited tantalum can occur in two different crystalline structures (α- or β-phase) in which the more conducting α-phase is preferred. The α-phase formation is strongly influences by the dielectric and the thickness and the stoichiometric of TaN. For the crystalline structure determination of tantalum various methods can be used. X-ray diffraction (XRD) measurements deliver the characteristic α- and β-tantalum phase reflexes (fig. 2a). As α-tantalum has a one order of magnitude lower resistivity it is also possible to distinguish them because of their different sheet resistivity for equal thick films measured by four-point probe (table 1). By the different progresses in intensities in the valence band, what can be determined in situ in the XPS (fig. 2), the tantalum phase can also distinguished. The maximum of the density of states in the valence band of the conductive α-phase is energetically lower and thus closer to the Fermi edge than the signal for the β-phase.

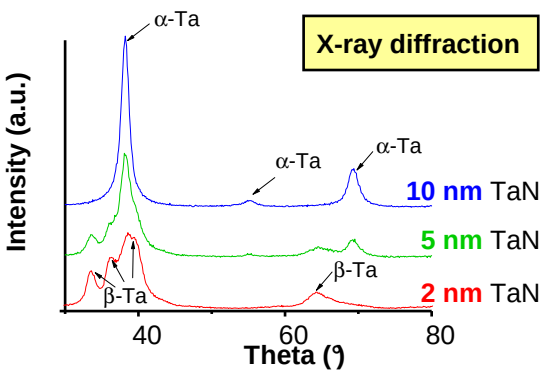
On sufficient thick tantalum nitride or nitrogen rich tantalum nitride as well as on porous SiCOH (ULK) the favored α-tantalum phase forms preferably. In figure 2, the influences of various parameters on the growth of the tantalum phase are visible. The reason for this seems to lie in the tantalum silicide concentration at the interface between TaN and dielectric.

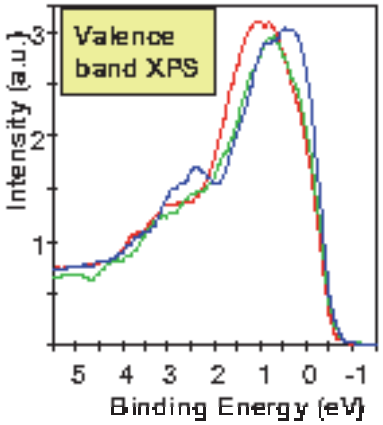
In 2009 this work was financed by the KUWANO (BMBF) and STRUCTURE (SMWK) projects.

(Lukas Gerlich)

Ta-Widerstand	
TaN (nm)	Rs (Ω)
0	89.9 →β
2	77.2 →β
5	37.2
10	16.5 →α
20	15.1 →α

1 *Table: Resistivity of 20 nm tantalum on different TaN-thicknesses on SiO_2*





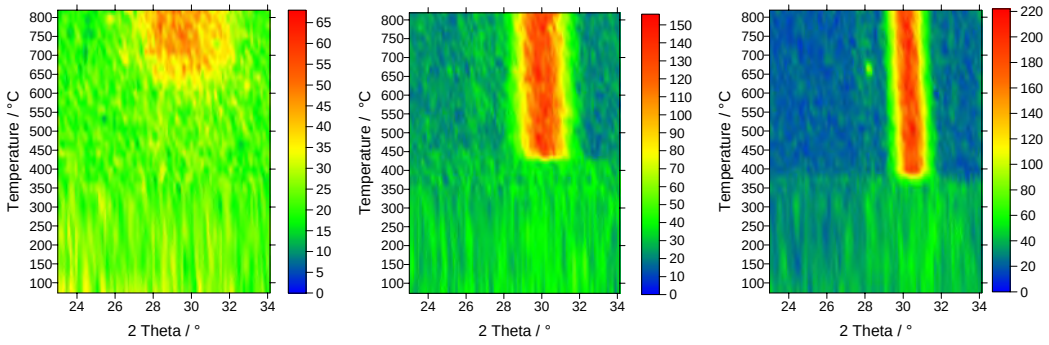
3 *XRD (a) and valence band XPS (b) of 20 nm tantalum on 2, 5 and 10 nm TaN on SiO_2.*

ANALYTICS

Investigations on crystallization of ultra thin high-k gate dielectrics

The optimization of the electrical properties of Hf-based high-k gate dielectrics (leakage) is done within the HEIKE project. Therefore, sample series with different stoichiometry (doping with a second metal oxide species) and different deposition conditions (ALD vs. MOCVD, different deposition temperatures) have been investigated. In order to generate thin film phase diagrams, additionally the thickness of the high-k layer was varied in the range between 2 - 6nm. The samples have been studied by means of grazing incidence XRD in the temperature range between 40°C – 780°C in nitrogen atmosphere.

As shown in earlier investigations on thickness depending crystallization of ZrO2 thin films, also for Hf-based films the crystallization temperature significantly depends on the film thickness. This is due to the rising influence of the surface energy over the bulk energy. In ALD deposited HfZrO4, the crystallization temperature increases from 380°C for 6nm layers and 440°C for 4nm thick layers to 660°C for 2nm thick layers (see Fig. 1). In the 6nm HfZrO4 film, additionally to the cubic phase, traces of a monoclinic phase are observed. The Hf richer the films are (at same film thickness), the higher temperatures for crystallization are needed. The influence of the deposition condition is such, that films deposited at lower temperature require higher annealing temperatures for crystallization.
(Dr. Lutz Wilde)



1 *Thickness depending crystallization of ALD deposited HfZrO4 films (left: 2nm, center: 4nm, right: 6nm)*

from left: Dr. Volkhard Beyer, Dr. Lutz Wilde, Prof. Peter Kücher, Dr. Christoph Hohle, Dr. Malte Czernohorsky

FUNCTIONAL ELECTRONIC MATERIALS

ALD process development for DRAM capacitors

Metallization process: Copper as a wiring material

Epitaxy processes for the application in CMOS technology

COMPETENCE AREA FUNCTIONAL ELECTRONIC MATERIALS

Development of Materials

Ziel der Forschungsarbeiten ist die Entwicklung von Materialsystemen mit optimierten dielektrischen Eigenschaften (High-K) für Anwendungen in nanoelektronischen Bauelementen. Der Schwerpunkt liegt dabei auf Transistoren und Speichern. Eine der Kernkompetenzen dabei ist die hochkonformale Atomlagenabscheidung (ALD) von dielektrischen und leitfähigen Schichten auf 300 mm Si-Wafern und anderer Wafer-Größen sowie die Metallisierung von Kupfer im Dual-Damascene-Verfahren für aktuelle und zukünftige BEOL-Technologiegenerationen.

Competence area
Functional Electronic Materials

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Group leader
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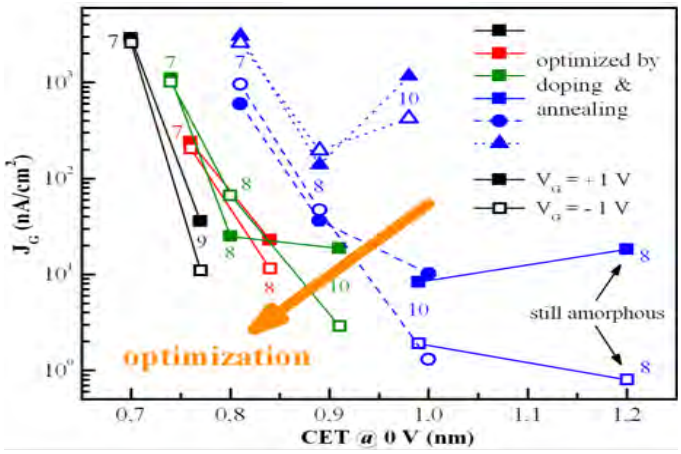
FUNCTIONAL ELECTRONIC MATERIALS

ALD: Process development for DRAM capacitors

Die Oberfläche des DRAM Speicherkondensator wird im Zuge der fortschreitenden Strukturverkleinerung mit jeder Technologiegeneration geringer. Deshalb müssen die als Speicherdielektrikum eingesetzten Materialien hinsichtlich ihrer Dielektrizitätskonstante (k) angepasst werden um eine ausreichende Kapazität für den zuverlässigen Betrieb zu erhalten. Die Materialienentwicklung für High-k-Dielektrika, die in MIM (Metall Isolator Metall) DRAM-Kondensatoren eingesetzt werden, führte über HfSiO/Al_2O_3 Systeme (k~10-25) in 70 nm Technologien zu ZrO_2/HfO_2 (k~40) in der 50 nm Generation. Der Trend zu höheren k-Werten wird fortgesetzt und wird schließlich zur Einführung von Ultra-high-k-Materialien (k > 50) mit Perowskitstruktur führen.
[ITRS 2009 Edition, www.itrs.net]

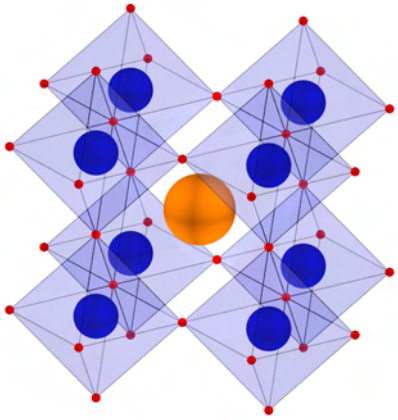
Am Fraunhofer CNT werden ALD-Prozesse zur Abscheidung von Al_2O_3, HfO_2 und ZrO_2 basierenden Materialien entwickelt, die die Anforderungen an DRAM-Kondensatoren erfüllen. Hierfür wurden sowohl industieerprobte Präkursoren wie Alkylamide als auch neu entwickelte mit Cyclopentadienyl-Liganden wie ZyALD (Air Liquide) untersucht. So wurde z. B. ein ZrO_2/Al_2O_3 Mischsystem optimiert, um die Anforderungen bezüglich Leckstrom und Kapazität für sub-50 nm Technologien zu erfüllen (CET<0.9 bei <1nA/cm2; Abb. 1).



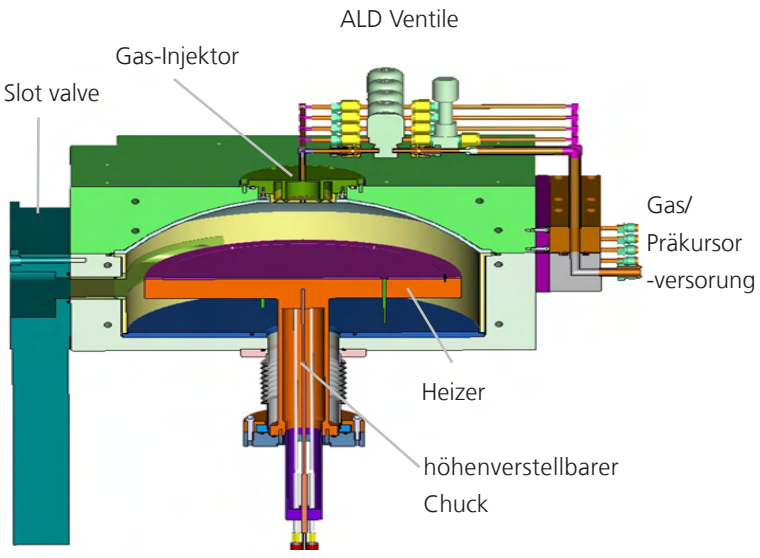
1 *CET-Leckstrom-Skalierung für DRAM-MIM-Kondensatoren unter Verwedung von ZrO_2, Al_2O_3 und SiO_2 Materialsystemes und TiN-Elektroden. [W. Weinreich, INFOS 2009]*

ALD-Abscheidung von $SrTiO_3$ Schichten

Strontiumtitanat ($SrTiO_3$) ist aufgrund der hohen spezifischen Dielektrizitätskonstante (k>100) ein Material, das als Speicherdielektrikum für zukünftige DRAM-Generationen in Frage kommt (Abb. 2). Um dieses Materialsystem in den heutzutage in der Halbleiterelektronik üblichen dreidimensionalen Strukturen abzuscheiden, sind ALD-Verfahren notwendig, da nur diese die notwendige Kantenbedeckung aufweisen. Für die Abscheidung von ternären Oxiden wie $SrTiO_3$ werden zwei ALD-Prozesse für die beiden binären Komponenten (SrO und TiO_2) verwendet, da keine ALD-Präkursoren verfügbar sind, die beide Metalle als Zentralatom enthalten. Die beiden Teilprozesse müssen ein gemeinsames Temperaturfenster aufweisen, um für die Abscheidung von $SrTiO_3$ kombiniert werden zu können. Am Fraunhofer CNT wurden Abs-Sr (Air Liquide) als Strontium-Präkursor sowie Star-Ti (Air Liquide) als Titan-Präkursor hinsichtlich ihrer Eignung zur ALD-Abscheidung von $SrTiO_3$ auf 300 mm Wafern unter Verwendung von Ozon als Oxidationsmittel evaluiert. Die Untersuchungen wurden auf einem 300 mm Single Wafer Tool, das aktuellen industriellen Fertigungsstandards entspricht, durchgeführt (Abb. 3).



2 *$SrTiO_3$ Kristallstruktur mit typischer Perowskit-Struktur*

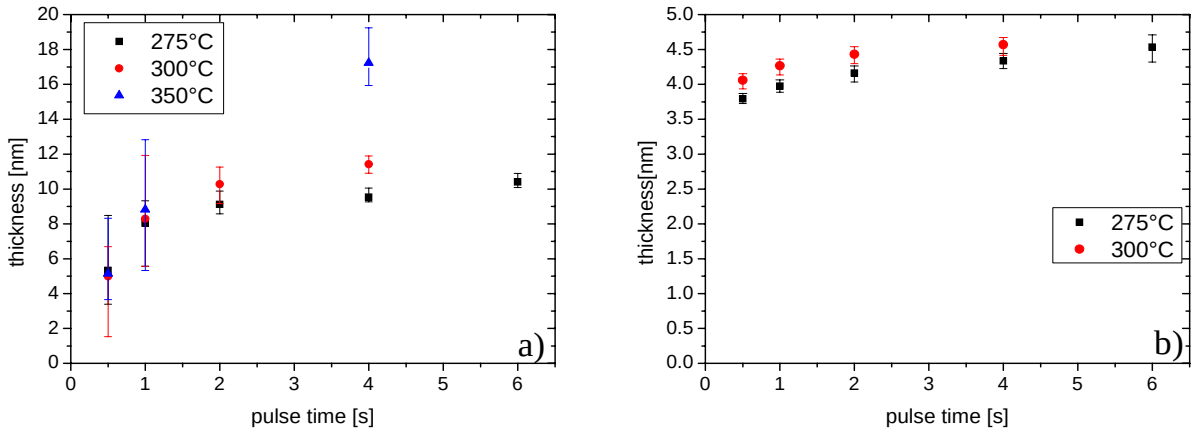


3 *Schema der verwendeten 300 mm Prozesskammer (Jusung Eureka 3000)*

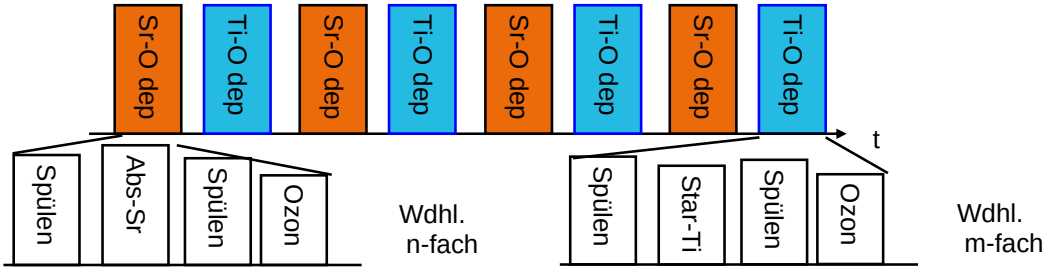
FUNCTIONAL ELECTRONIC MATERIALS

Hierzu wurden zunächst Prozessfenster für die binären Verbindungen (TiO_2 und SrO) ermittelt.
Exemplarisch sind in Abb. 4 Sättigungskurven für Star-Ti und Abs-Sr dargestellt. Beide Präkursoren weisen bis 300 °C eine, für ALD-Prozesse typische Sättigung mit der Pulszeit auf. Bei höheren Temperaturen kommt es zur Dekomposition des Strontium-Präkursors.

Da beide Präkursoren bis 300 °C selbstlimitiert wachsen, sind ALD-Abscheidungen von Strontiumtitanatschichten mit diesen beiden Präkursoren möglich. Nach der Untersuchung der reinen binären Oxide wurden Mischungen der beiden Komponenten abgeschieden, um zu untersuchen inwieweit die Schichtstöchiometrie kontrolliert werden kann. Hierzu wurden n SrO Zyklen gefolgt von m TiO_2 Zyklen abgeschieden, um die Schichtzusammensetzung zu variieren. Die Anzahl der Wiederholungen dieses Subzyklus (m+n) bestimmt die Schichtdicke (Abb. 5).



4 *A) Sättigungskurven für Abs-Sr a) und Star-Ti B) Die Schichtdicke wurde per Ellipsometrie bestimmt.*



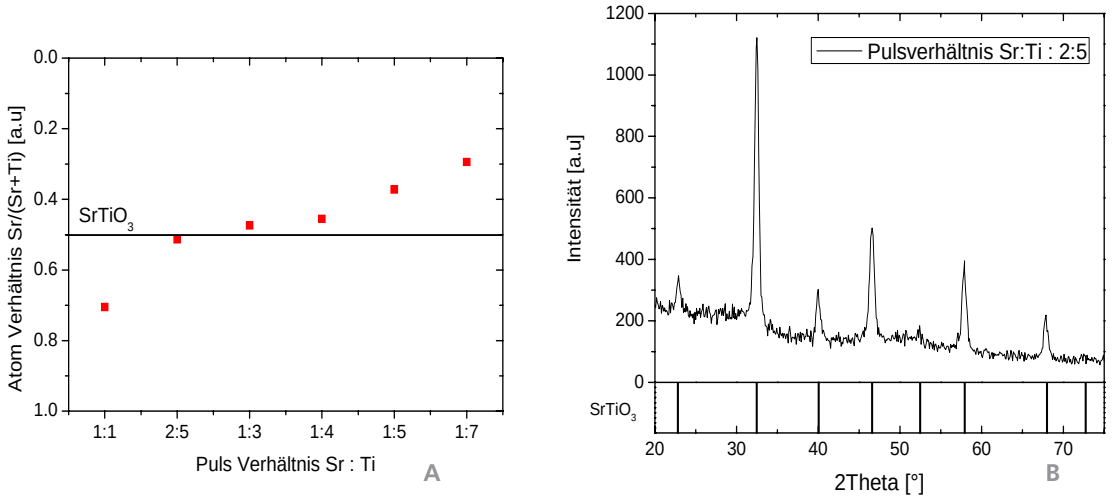
5 *Pulsschema für die Abscheidung von SrO/TiO_2 Mischschichten*

Die Zusammensetzungsanalyse (Abb. 6a). zeigt, dass für ein Pulsverhältnis zwischen 2:5 und 1:3 annähernd ein Sr/(Sr+Ti) Atomverhältnis von 0,5 erreicht wird. Die Schichten wurden nach der Abscheidung einem RTP-Temperung in N_2 Atmosphäre bei 650 °C unterzogen, um die nach Abscheidung amorphe Schicht auszukristallisieren. Ein anschließend unter streifendem Einfall aufgenommenes Röntgendiffraktogramm zeigt die für kubisches $SrTiO_3$ charakteristischen Peaks (Abb. 6b).

Damit konnte gezeigt werden, dass es mit den beiden verwendeten Präkursoren möglich ist $SrTiO_3$ Schichten zu erzeugen, die nach einem Kristallisationstemperung die kubische STO-Phase zeigen. Diese weist die höchste Dielektrizätstkonstante des $Sr_xTi_yO_z$ Materialsystems auf.

Ausgehend von den bisherigen Untersuchungen sollen im nächsten Schritt Abscheidungen auf Metallelektroden durchgeführt werden, um die Schichten elektrisch zu charakterisieren. Des weiteren soll das Wachstumsverhalten der beiden Komponenten auf verschieden Oberflächen und Substraten genauer charakterisiert werden.

(Dr. Jonas Sundvist, Stefan Riedel)



6 *A) Zusammensetzung der STO-Schichten* *B) Röntgendiffraktogramm der kristallisierten Schichten*

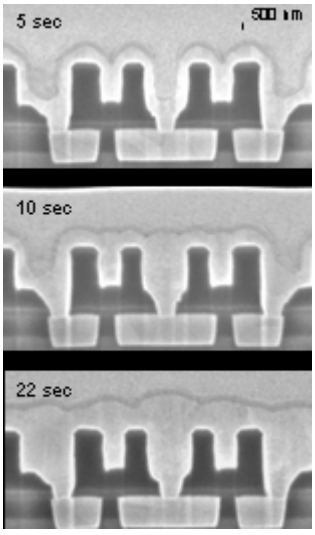
FUNCTIONAL ELECTRONIC MATERIALS

Metallization process: Copper as a wiring material

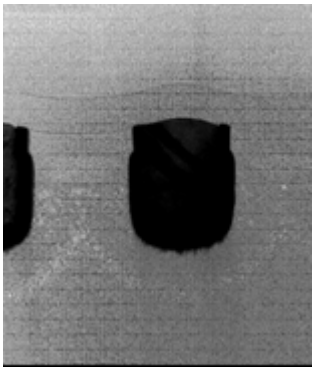
The use of copper in the semiconductor industry as a wiring material revolutionized the metallization process and contributed substantially to launch faster, smaller and less energy consuming processors.
On one hand, this progress can be attributed to changed process technologies, which allow producing more complex multilayered interconnects; and on the other hand to the electrical properties of copper itself which lead to processor performance improvement. Compared to 5 years ago, modern processors contain three to ten times more transistors on the same area without increased energy consumption. In order to keep up with this rapid progress, new processes and new materials have to be studied and developed. Thus, a brief insight into the research fields of the Fraunhofer CNT under the project lead of GLOBALFOUNDRIES in the area of copper metallization will be given.

About the copper super fill behavior

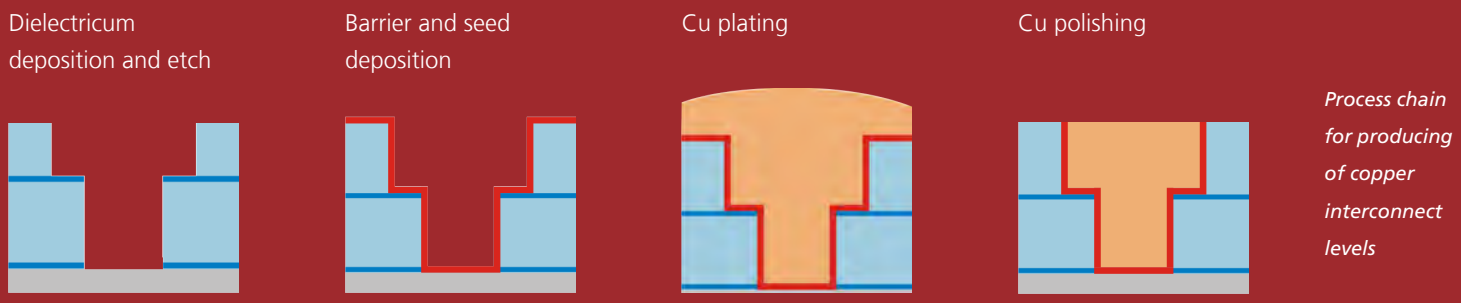
The electrochemical deposition of copper films is an established process for the production of ultra-pure crystalline copper for various industrial applications. Copper plating is also the process of choice for producing copper interconnects in integrated circuits. The reason for that is the so-called 'super filling'. Super filling describes the void-free structure filling from the feature bottom towards the feature top. This is enabled by adding organic electrolyte additives. Furthermore, the additives are responsible for a defect-free polycrystalline texture and a nearly perfect leveling of the growing copper film surface.
From the technological point of view, it is important to adapt the plating process efficiently to progressively decreasing interconnect dimensions and to enhance the electrical and mechanical properties of the copper lines.



1 *Kupferabscheidung: "Superfill"-Verhalten: Hohlraumfreies Auffüllen der Strukturen mit Kupfer (Quelle: GLOBALFOUNDRIES Dresden Module One LLC & Co. KG)*



2 *Kupferisolierung: SEM-Querschnitt durch eine eingekapselte Kupferlinie in porösem Dielektrikum. Der weiße Rand unter der Kupferlinie markiert den Ätzschäden, der zur Degradation der dielektrischen Eigenschaften führt (Quelle: GLOBALFOUNDRIES Dresden Module One LLC & Co. KG)*



Process chain for producing of copper interconnect levels

New materials for copper isolation

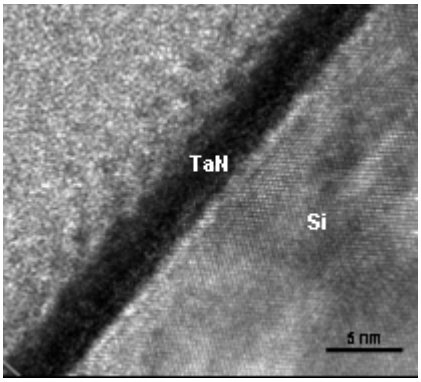
The copper wiring is embedded into a dielectric material, which is responsible for the mechanical stability of the interconnects and the electrical insulation between adjacent copper lines. Currently, carbon doped SiO2, so called SiCOH, is used. However, to achieve even more compact wiring structures for more powerful processors, the capacitance between the copper wires must be further reduced. Hence, there is a tendency of integrating nano pores into the SiCOH film. The integration of nano porous materials is a technical challenge due to the high sensitivity to etch and cleaning processes. Patterning with high energetic ion bombardment damages the surfaces, which results in a decreased electrical isolation. Therefore, intensive research is carried out to investigate feasible surface treatment and sealing processes.

Integration and Reliability Tests

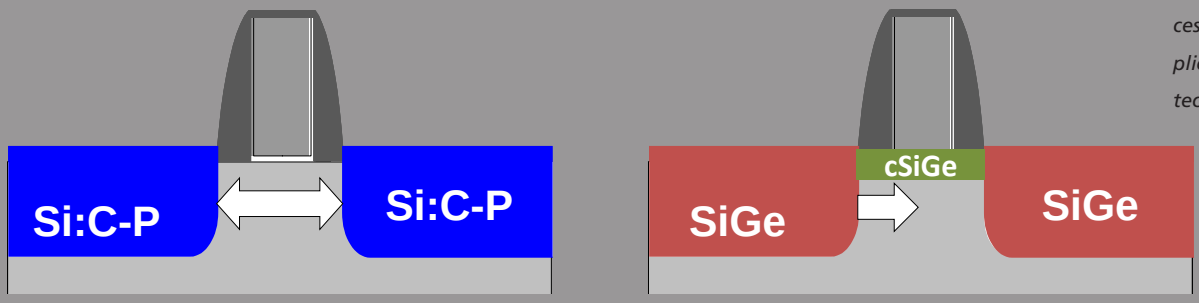
Small changes in material properties are influencing the performance and power consumption of processor dies. To minimize stresses, the interactions of dielectric, barrier layer and copper have to be characterized. Stress migration tests help to identify weak points and are used to optimize process steps. Even with ever shrinking structures and an increasing complexity of process technologies the reliability of devices has to be guaranteed. sein. *(Romy Liske, Thomas Oszinda, Lukas Gerlich)*

Evaluating new process technologies

A barrier layer between the dielectric material and the embedded copper prevents the copper from diffusing into adjacent materials. The quality requirements for barrier layers are high. For instance, a strong adhesion of the barrier layers to both the dielectric and copper without forming alloys is required. At the same time, barrier films need to be as thin as possible. A TaN/Ta double layer, deposited by a PVD process (PVD - physical vapor deposition), was found to be an optimal system fulfilling those demands. Difficulties may arise when the feature sizes become smaller and smaller, as it gets harder to achieve thin and conformal layers inside high aspect ratio features with PVD. Therefore, the evaluation of other deposition techniques and alternative barrier materials is in progress.



3 *Barriereschichten: TEM-Aufnahme einer amorphen, mittels ALD abgeschiedenen, 4 nm dünnen TaN-Schicht auf Si (Quelle: GLOBALFOUNDRIES Dresden Module One LLC & Co. KG)*



1 *Epitaxy processes for the application in CMOS technology*

Epitaxy processes for the application in CMOS technology

At Fraunhofer-Center Nanoelectronic Technologies, epitaxy processes for the application in CMOS technology are studied. One main topic is the deposition of Si1-xCx layers for the generation of mechanical stress in future nMOS transistors. Via heteroepitaxy of Si1-xCx layers which have a smaller lattice parameter compared to silicon, the electron mobility of nMOS transistors increases according to the effect of piezo-resistance. The research focuses on the deposition of layers via LP-CVD, the study of thermal stability and the evaluation of the stressor in product wafers in cooperation with Globalfoundries Module One LLC & Co. KG, Dresden. Due to the low solubility of carbon in silicon, the deposition of metastable, defect free epitaxial layers is a challenging task. Nevertheless it is possible to grow highly strained layers with 2 at.% carbon. The characterization of the epitaxial films on 300 mm Silicon wafer is done by high resolution X-ray diffraction (HR-XRD) using an inline tool. For the investigation of the thermal stability of the layers, a lab furnace enabling rapid thermal anneals is available, which is used to analyze the temperature and time dependent stress relaxation under Ar, N2 oder N2O2 ambient.

Additionally Fraunhofer CNT studies in collaboration with Globalfoundries the integration of silicon germanium (SiGe) as channel material in pMOS transistors for the 32nm technology node. SiGe has a different band gap compared to silicon. Thus, the use of SiGe in the transistor channel is of interest due to the possibility to adjust the threshold voltage (VT) of the transistor independently of the gate stack and to enhance the hole mobility. A VT difference of about 300 mV has been reported for a germanium concentration of 30 at.%. However, the germanium atoms localized at the interface between semiconductor and gate oxide lead to an increased number of interface states. SiGe as transistor channel material causes also a larger semiconductor capacitance, which has an unfavorable influence on the CET value of the gate stack. Besides the application as channel material a well established technique is the so called "embedded SiGe". SiGe generates mechanical strain from the source/drain regions towards the p-channel transistor (s.Fig.XX). Due to the piezo-resistance effect a significantly enhanced charge carrier mobility can be achieved. Thus, in high performance CMOS devices it is favorable to use SiGe both as stressor and as channel material in the same transistor. But at very small dimensions of short channel transistors the strain from the SiGe channel counteracts the strain from the embedded SiGe. This reduces the uniaxial strain generated in the transistor channel which yields a reduced enhancement of the charge carrier mobility by embedded SiGe. It was shown, that this competing effect can be minimized by optimizing the layer thickness of the SiGe channel.

(Ina Ostermay, Andreas Naumann)

DEVICES & INTEGRATION

Development of future non-volatile memories

Entwicklung hochselektiver Ätzverfahren

CMP modeling of dielectric materials

COMPETENCE AREA DEVICES & INTEGRATION

Development and integration of nanoelectronic devices

The main research topic of the competence group „Device & Integration" is the development and integration of nanoelectronic devices. Furthermore the main focus is on the electrical characterization of semiconductor devices on wafer level such as memory devices (single memory transistors, arrays, and demonstrators) as well as the development of concepts for the integration of new materials and innovative etching processes in process flows in order to fabricate nanoscaled structures. This work is assisted by simulations on device and process level.

Competence area
Devices & Integration

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Devices & Integration

DEVICES & INTEGRATION

Electrical characterization and development of materials and processing technologies for future non-volatile memories

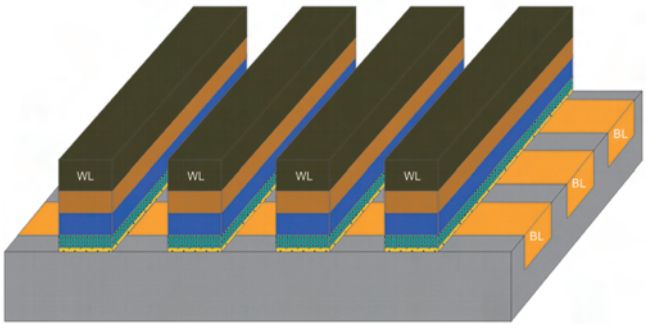
Data storage solutions such as embedded or stand-alone Flash but also Flash-based systems like solid-state drives require comprehensive characterization and test of large memory arrays in order to meet the high product reliability targets. Stable manufacturing processes are a precondition for a high number of storage cycles, long data retention, high data throughput, and a reliable operation of the device or product.

Equipped with state-of-the-art unit-process equipment and powerful memory testing systems Fraunhofer CNT with its experienced and international networked team offers an outstanding platform to support industrial customers in the introduction and characterization of new materials and processes that are used e.g. in memory products with low internal voltages. In particular unit-processes for the atomic layer deposition (ALD) of high-k dielectrics as well as for special etching methods and a large variety of analytic equipment (e.g. XRD, TEM, SIMS) are available to achieve a deeper understanding for the development of structures and layers in the nanometer-scale.

Fully automated electrical characterization and flash test systems in combination with powerful and flexible data processing enable a fast characterization of large memory arrays. It is possible to perform the electrical measurements on wafer-level (up to 300mm) as well as on packaged components.

The development of non-volatile memories for next technology nodes towards smaller features sizes implies increasing efforts to achieve reliable memory cells.

On the one hand continuously scaled memory cells require less and less charge carriers for information storage. On the other side the relevance of cell cross-talk and disturb effects of adjacent cells increases at smaller distances. Moreover thinner dielectrics provoke a higher charge carrier leakage from storage layers. The next section reports from an actual research topic at Fraunhofer CNT, the development of charge trap based memory devices (TANOS cell concept). A TANOS cell consists of a stack of different materials as illustrated in Fig. 1.



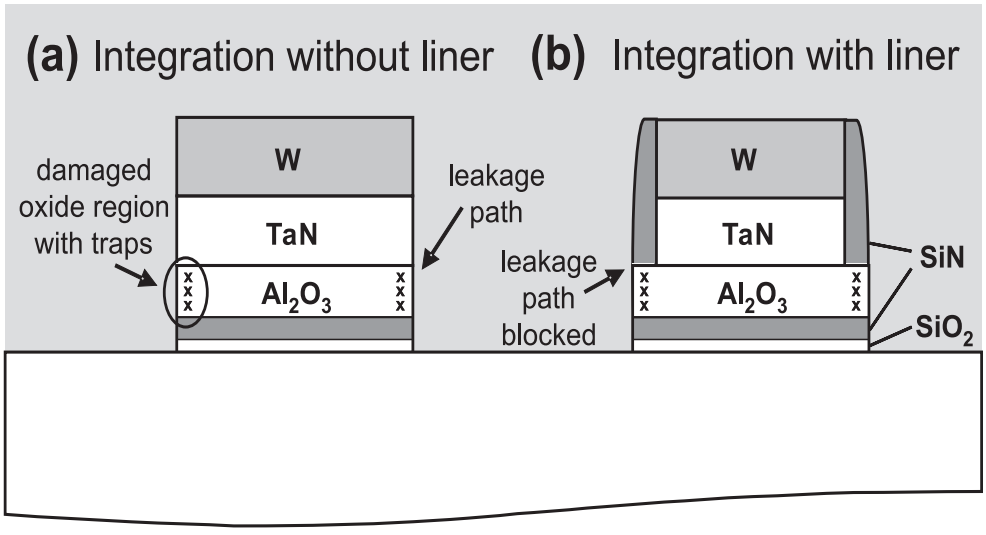
1 *Schematic of a TANOS stack (TaN/Al_2O_3/Si_3N_4/SiO_2/Si). The charge is stored within the silicon nitride (Si_3N_4) layer.*

Encapsulation Liner

One of the technology problems Fraunhofer CNT was facing in the framework of the joint European research project GOSSAMER during the development of the TANOS cells was the insufficient data retention and write/erase-performance of the memory devices.

The root-cause of this behavior was identified as a structural damage at the sidewalls of the TANOS cells which occurs during the reactive ion etching process of the total layer stack. Defects at the sidewall of the Al_2O_3 blocking oxide created by this etch treatment induce the formation of leakage pathways between gate electrode and nitride storage layer (Fig. 2a).

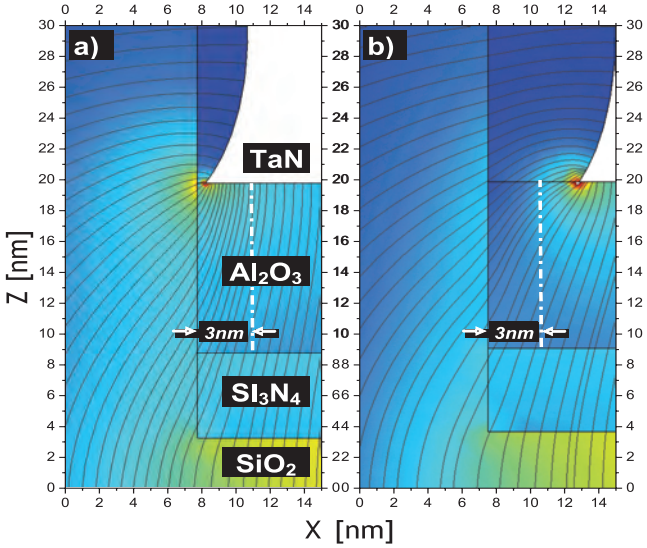
This causes a considerable charge loss from the storage layer during the data retention test. In order to eliminate this effect the so-called "encapsulation liner" concept was developed. Due to the deposition of a thin Si3N4 layer (liner) after etching the TaN metal layer, the damaged region of the Al2O3 blocking oxide is electrically separated from the gate electrode (Fig. 2b). An exchange of charge carriers between control gate and storage layer through the defective sidewall areas is effectively suppressed. Electrical characterization showed an overall improved performance of the TANOS cells revealing better data retention (reduced charge loss) and a clearly enhanced write/erase speed (see Fig. 3a).



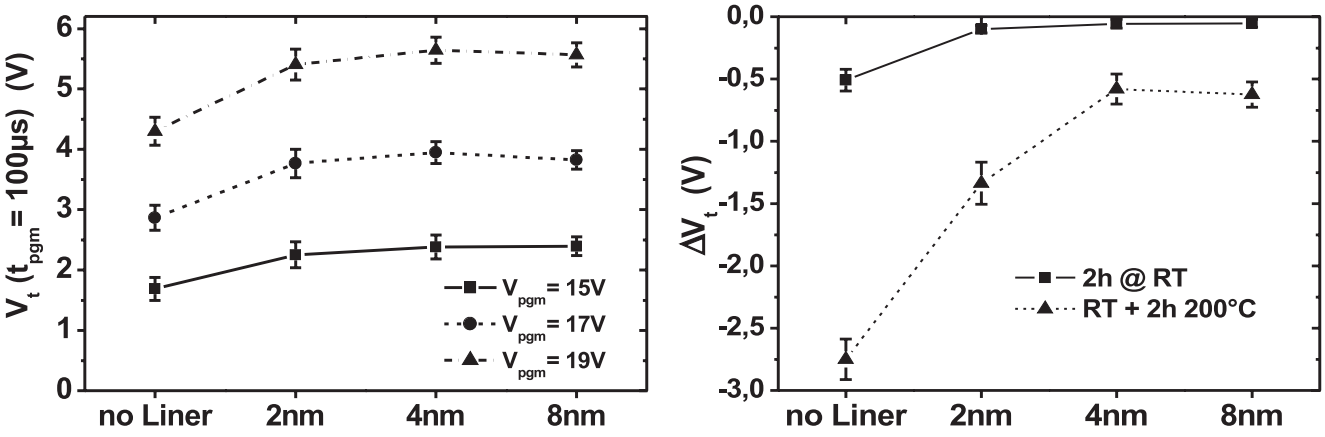
2 *Schematic of a TANOS memory cell without encapsulation liner (a) and with liner (b). Integrating the Si_3N_4 deposition the leakage path through the Al_2O_3 blocking oxide is disconnected.*

DEVICES & INTEGRATION

Besides extensive electrical and physical analysis, Fraunhofer CNT used state-of-the-art simulation software to determine the distribution of electric fields within the device to gain a deeper understanding of the mechanisms leading to the observed behavior. In the simulation the electrostatic fields were calculated for the TANOS stack with and without encapsulation liner for both at program and erase conditions using the finite elements method. As shown in Fig. 4 the simulation confirms the hypothesis that the damaged sidewall of the Al_2O_3 layer in coincidence with enhanced electrical fields along the bottom edge of the gate electrode is responsible for the generation of the leakage pathways. The beneficial effect of the encapsulation was observed to be dependent on the thickness of the deposited layer. As shown in Fig. 3 the effect saturates with no further improvement at a liner thicknesses of about 4 nm. This observation confirms the hypothesis that the defective region of the blocking oxide sidewall reaches a depth of approximately 3 nm. .
(Raik Hoffmann, Daniel-André Löhr)



4 *Simulations of the static electrical field in the interface regions between gate dielectric, blocking oxide, and storage nitride layer during erase of the TANOS cell.*



3 *Results of the electrical characterization (a) of program trends and (b) of data retention for several liner thicknesses. During programming the cell featuring the encapsulation liner achieves a larger shift of the threshold voltage (Vt) applying the same programming time and voltage.*

Hochselektive Ätzverfahren zur Herstellung dreidimensionaler Strukturen

Die Entwicklung hochselektiver Ätzverfahren zur Herstellung von Strukturen mit unterschiedlich hohen Aspektverhältnissen (1:1 bis 1:10; Aspektverhältnis = Strukturbreite/Strukturtiefe) steht seit vielen Jahren im Fokus der Halbleiterindustrie und ist ein wesentliches Arbeitsgebiet des Fraunhofer CNT.

Eine besondere Herausforderung für die Entwicklung dieser Strukturierungsprozesse ist eine geometrieunabhängige Einsetzbarkeit, d. h. es sollen kritische kleinste Strukturbreiten (<50 nm) bis hin zu Mikrometer (>>10 µm) großen Strukturen mit vergleichbaren Aspektverhältnissen hergestellt werden. Das ermöglicht es mit einem Ätzprozess verschiedene Anwendungen in der Mikroelektronik (Graben- und Kontaktätzungen z. B. für CMOS und DRAM), Mikrosystemtechnik (MEMS) sowie der 3D Systemintegration (Through Silicon Via (TSV)) zu adressieren.

Das Fraunhofer CNT verfolgt in diesem Zusammenhang unterschiedliche Entwicklungsthemen der Nanostrukturierung. Einerseits wurden effektive Passivierungsprozesse zur Herstellung von Grabenstrukturen in Silizium untersucht. Andererseits wurde ein innovatives Hartmaskenkonzept entwickelt, um deutliche Selektivitätsverbesserungen erreichen zu können. Diese Technologien verstehen sich als allgemeine Prozessierungsverfahren, die sich auch auf andere Strukturierungsanforderungen bzw. Materialschichtsysteme übertragen lassen.

Die Herstellung von dreidimensionalen Strukturen in Silizium oder anderen Schicht- bzw. Materialsystemen basiert auf einem komplexen Zusammenspiel sehr unterschiedlicher Prozesse. Die Strukturierungsabfolge startet in aller Regel mit einem fotolithografischen Prozess. Es wird eine Vorlage zur weiteren Strukturierung in einem Fotolack erzeugt, wobei die fortschreitende Miniaturisierung die Fotolithografie vor stetig wachsende Anforderungen stellt. Die Entwicklung bedingt die weitere Reduzierung der Fotolackdicke, um eine Auflösung von Strukturen, die kleiner als 50 nm sein sollen, noch gewährleisten zu können. Tendenziell wird die Lackdicke für zukünftige Technologieknoten deutlich unter 100 nm sinken.

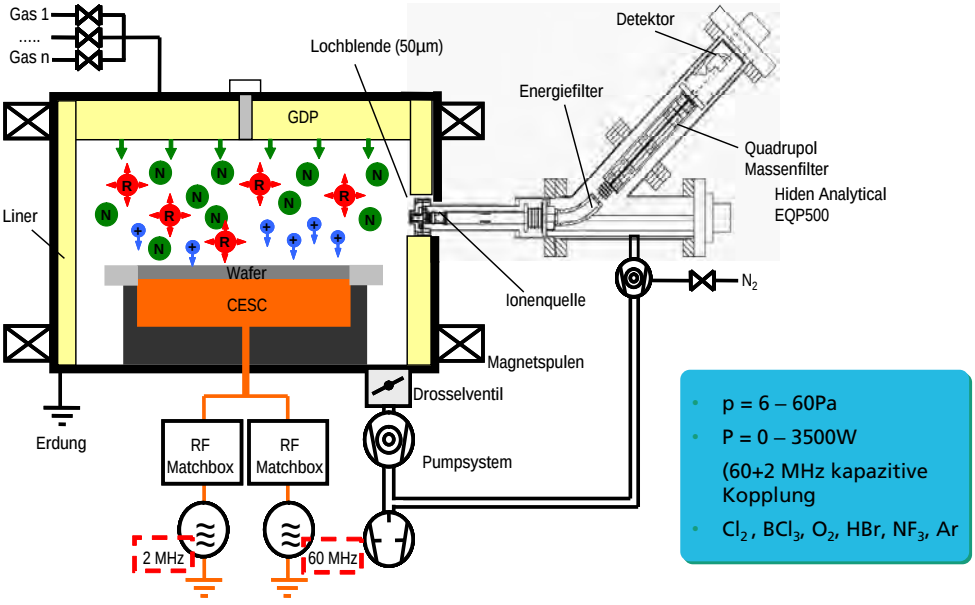
Die Übertragung der erzeugten Lackstrukturen in den Siliziumwafer (oder eine andere Materialebene) erfolgt üblicherweise im Trockenätzverfahren. Auch diese Prozesse unterliegen einer stetigen Weiterentwicklung und Optimierung infolge der Miniaturisierung. Beispielsweise bieten dünne Fotolacke immer weniger Stabilität während der Trockenätzung, was die Erzeugung von Strukturen mit hohen Aspektverhältnissen deutlich erschwert. Aufgrund der im Allgemeinen eher geringen Selektivität des Lackes zur zu strukturierenden Unterlage können nur noch sehr dünne Schichten geätzt werden. Die Einführung einer sogenannten Hartmaske bietet hier Abhilfe. Vor der lithographischen Prozessierung wird über die eigentlich zu strukturierende Materialschicht eine weitere dünnere Schicht aufgebracht, die sog. Hartmaske. Diese ist in ihren Eigenschaften so ausgewählt, dass sie auch über einen sehr dünnen Fotolack noch gut zu strukturieren ist und für die folgenden Ätzprozesse eine ausreichend hohe Selektivität bereitstellt.

DEVICES & INTEGRATION

Innovative Strukturierungsprozesse am Fraunhofer CNT

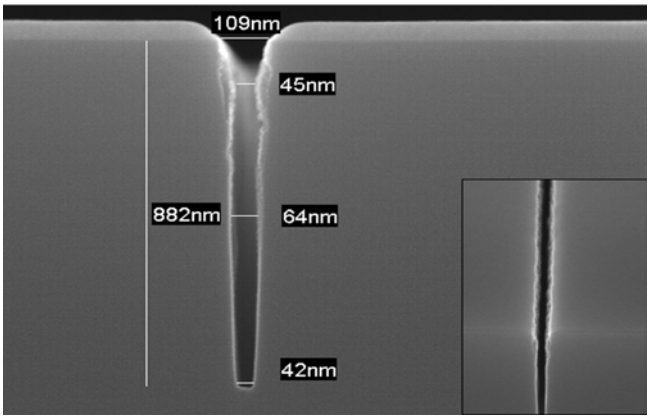
Ein konventionelles Hartmaskenmaterial ist SiO_2, wobei je nach Anwendung Schichtdicken von 400 bis 800 nm auf das zu strukturierende Substrat aufgebracht werden. Das Fraunhofer CNT arbeitet standardmäßig in der E-Beam Lithografie mit Fotolackschichtdicken zwischen 80 und 150 nm. Diese Lackschichtdicken reichen allerdings nicht mehr aus, um konventionelle SiO_2 Hartmaskendicken (> 400 nm) strukturieren zu können. Aus diesem Grund arbeitet das Fraunhofer CNT an hochselektiven Ätzprozessen, um auch weiterhin in der konventionellen Strukturierungsabfolge mit dünnen Fotolacken (100 - 130 nm) arbeiten zu können.

So konnten Silizium-Strukturen mit einer Tiefe von 50 bis 1500 nm unter Verwendung einer 100 nm dicken SiO_2 Hartmaske erzeugt werden. Die eingesetzte Ätzkammer ist ein Parallelplattenreaktor, der die Prozessierung von 300 mm Si Wafer ermöglicht. Diese magnetisch verstärkte reaktive Ionenätzkammer (MERIE) ist mit zwei RF-Anregungsquellen (60 und 2MHz) ausgestattet (Abb. 1). Die erreichten Ätzraten liegen zwischen 1,1 und 1,7 µm/min bei einer Selektivität zum SiO_2 zwischen 20:1 und 60:1.

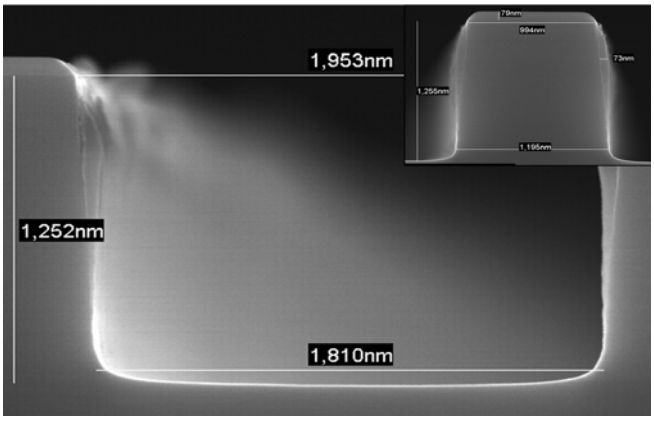


1 *Schema der Siliziumätzkammer mit angeschlossener Plasmaanalytik.*

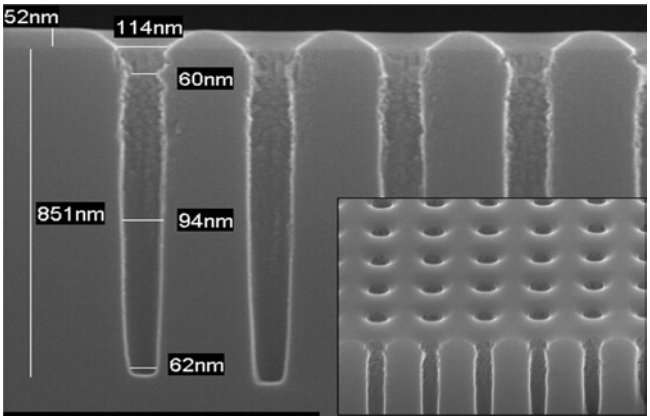
Wie in den Abbildungen 2 bis 5 dargestellt, können mit diesem Prozess für unterschiedliche Anwendungsgebiete Strukturen in einem weiten Größenbereich erzeugt werden.



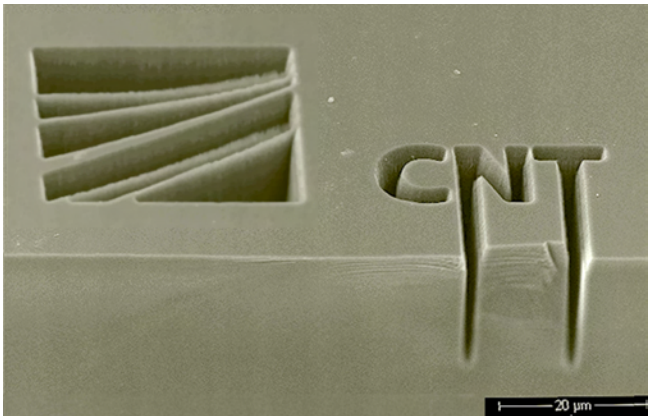
2 *SEM Abbildung der Bruchkante eines geätzten 60 nm dünnen Grabens.*



3 *SEM Abbildung eines 2 µm weit geätzten Grabens entlang einer Bruchkante.*



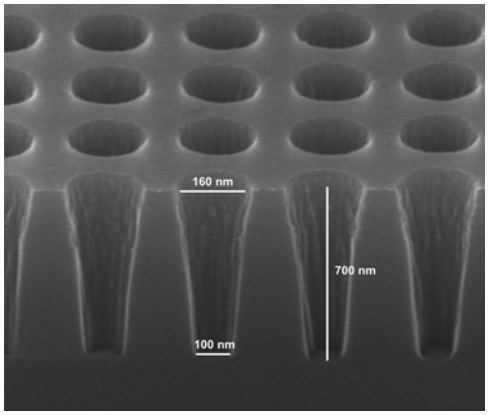
4 *SEM Abbildung eines Feldes mit 60 nm kleinen und 850 nm tiefen Löchern in Silizium. Der helle Kontrast an den Seitenwänden zeigt die homogen aufgebaute Passivierung.*



5 *SEM Abbildung des Logos des Fraunhofer CNT im Mikrometermaßstab bei gleichzeitiger Ätztiefe von ca. 20 µm.*

DEVICES & INTEGRATION

Einen weiteren Schwerpunkt der Arbeiten am Fraunhofer CNT stellt die Entwicklung neuartiger Hartmaskenkonzepte basierend auf ultradünnen Schichtstapeln für hochselektive Ätzverfahren dar. Ziel dieser Arbeit ist es, sehr hohe Aspektverhältnisse flexibel in unterschiedlichen Schichtstapel realisieren zu können ausgehend von sehr dünnen Fotolackdicken. Zur Herstellung von Löchern und Grabenstrukturen mit einer Tiefe von ~700 nm wurde ein Hartmaskenstapel bestehend aus zwei sehr dünnen Materialschichten genutzt (Abb. 6). Der Abtrag der Hartmaske betrug während der Ätzung lediglich 3 bis 5 nm bei einer mittleren Ätzrate von ca. 1 µm/min. Der geringe Abtrag zeigt, dass mit diesem Konzept hochselektive Ätzprozesse (Selektivität >60:1) realisiert werden können, wie sie mit konventionellen Hartmasken nicht zu erreichen sind. Die Übertragung dieses Strukturierungskonzeptes auf andere Materialsysteme eröffnet eine Fülle weiterer Anwendungsgebiete.
(Jan Paul)



6 *SEM Abbildung eines Löcherfeldes 160 nm kleiner und ~ 700 nm tiefer Strukturen, welches unter Einsatz des innovativen Hartmaskenstapels geöffnet wurde.*

Modeling and simulation of physical effects occurring during chemical mechanical planarization of dielectric materials

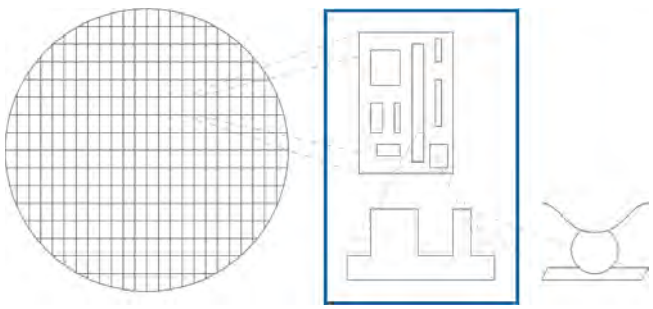
Highly integrated semiconductor products, like logic or memory chips, consist of multiple material layers. In the course of production the surfaces have to be planarized, i.e. brought to the same height level, over and over again to achieve sufficiently big process windows for critical steps like lithography or dry etching. Furthermore, planarization makes sure that defined structure sizes are obtained, thus eventually electrical components function.

The chemical mechanical planarization (CMP) is the current method of choice to achieve the demanded planarity. In CMP the wafer is attached to a rotating carrier and forced down onto an also rotating platen with CMP pad, such that a relative velocity between wafer and pad exists. As a result of the motion an added slurry is delivered into the gaps between wafer and pad. There together the slurry and the roughened pad become chemically and mechanically active which results in a removal of wafer material. The pad properties, e.g. the roughness, are kept constant through a conditioning process.

In the joint research project SIMKON, funded by the Federal Ministry of Education and Research, the modeling of CMP for dielectric materials, as used in inter-layer dielectric and shallow trench isolation processes, is advanced at the Fraunhofer CNT. It is the objective to improve the process understanding to be able to conduct simulations on feature and chip scale (Fig. 1).

The models and simulations respectively can be used to better control and optimize processes. By means of tailored CMP processes, especially with matched consumables, it is possible to reduce the high cost of ownership, which is crucial in mass production. On the other hand the ultimate goal for CMP modeling and simulation is to supply information about the manufacturability of a chip design before the production process has started. This way design rules and strategies could be given. Time and costs could be cut especially in the foundry business or in the production of small quantities and frequently changing chip layouts.

Until now the main focus has been put on the modeling of physical effects at the Fraunhofer CNT. On one hand the works concern the feature scale where the polishing pad roughness parameters are incorporated. On the other hand this concerns the chip scale. In this modeling approach long range interactions between structures in connection with the pad elasticity are considered.

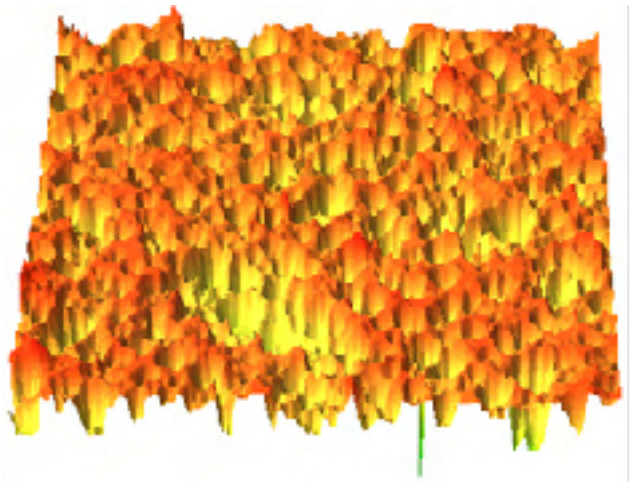


1 *from left to right – wafer, chip and feature, particle scale*

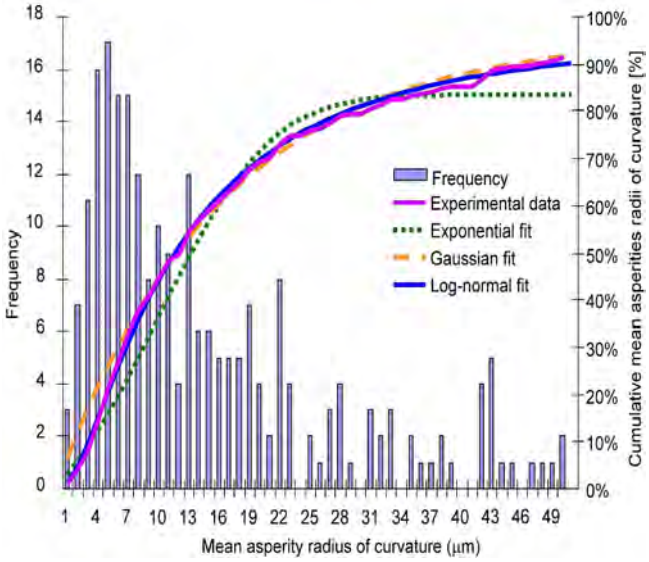
DEVICES & INTEGRATION

Examination of the conditioner influence on the pad roughness

From current knowledge it becomes obvious, that a better characterization of the polishing pad surface, especially a better methodology, is strongly needed to be able to better describe the complex interrelation of conditioning, pad roughness as well as removal rate, homogeneity and actual way of removal on patterned wafers. Based on this idea an analysis algorithm has been developed that extracts important tribological parameters from pad characterization data. Thereby high resolution 3D-images (Fig.2) of the polishing pad surface are processed with mathematical routines to detect, for example, height and size distributions (Fig.3) of the pad asperities as well as their respective area fraction. The thus obtained data are used in the projects modeling tasks at the feature level.
(Sascha Bott, Boris Vasilev)



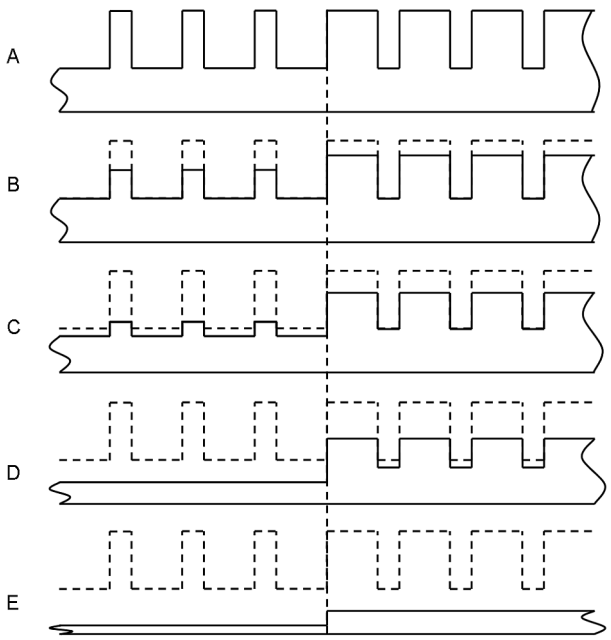
2 *3D-image of a polishing pad surface (1 x 1 mm²)*



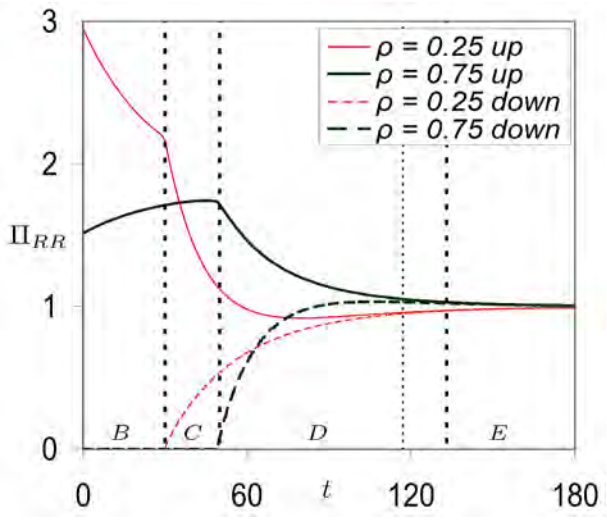
3 *Measured logarithmic normal distribution of the asperity radii of curvature for a certain height level*

Einbeziehung globaler Wechselwirkungen auf Chipebene

Nach dem Stand der Forschung beruht die Planarisierungswirkung beim CMP in wesentlichen Teilen darauf, dass auf exponierte Gebiete ein höherer Druck ausgeübt wird als auf zurückgezogene. Wesentliche strukturelle Parameter, die diese inhomogene Druckverteilung bestimmen, sind zum einen die lokale Strukturdichte, deren Einfluss bislang in der Literatur hauptsächlich betrachtet wurde. Des Weiteren ist bekannt, dass lokale Strukturen über Distanzen im Millimeterbereich miteinander wechselwirken, wodurch die gewünschte globale Planarisierungswirkung gewährleistet wird. Phänomenologische Ansätze, diese langreichweitigen Wechselwirkungen zu berücksichtigen, wurden im Fraunhofer CNT weiterentwickelt, so dass nunmehr neben der Strukturdichte auch die Höhe der einzelnen Strukturen, welche sich im Verlauf des CMP-Prozesses dynamisch verändert, Eingang findet.



4 *Strukturen mit unterschiedlicher Strukturdichte und deren zeitlicher Abtrag durch CMP (zeitlicher Verlauf von A nach E)*



5 *Qualitativ verbesserte Beschreibung der Abtragsraten an den Stegen (up) und Gräben (down) zweier angrenzender Gebiete mit 25 % und 75 % Strukturdichte (vgl. Abb. 4)*

PATTERNING

Nano-Interconnects and MEMS/NEMS via electron beam lithografie

Resolution limits in electron beam lithography

COMPENTENCE AREA PATTERNING

Flexible structuring beyond 50 nm vie electron beam lithography

Das Kompetenzgebiet Strukturierung beinhaltet die Herstellung von Resistmasken in speziellen Fotoresists mit Strukturgrößen bis 35 nm und deren Transfer in die darunter liegende Hartmaske. Belichtet wird mit der maskenlosen Elektronenstrahllithografie (E-Beam). Der Fokus im Kompetenzgebiet Strukturierung liegt auf der Bereitstellung von kunden- und anwendungsspezifischen Designs und Layouts auf 200 mm und 300 mm Wafern über ein modernes und flexibles Direktschreibverfahren.

Competence area
Patterning

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Group leader
Patterning

PATTERING

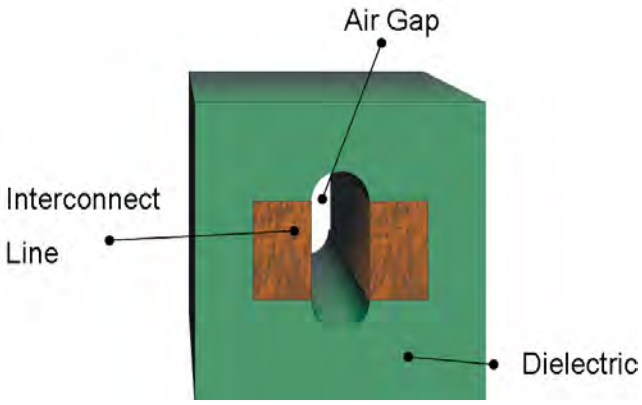
Nano-Interconnects and MEMS/NEMS via electron beam lithografie

Leitbahnstrukturen für Interconnectsystem

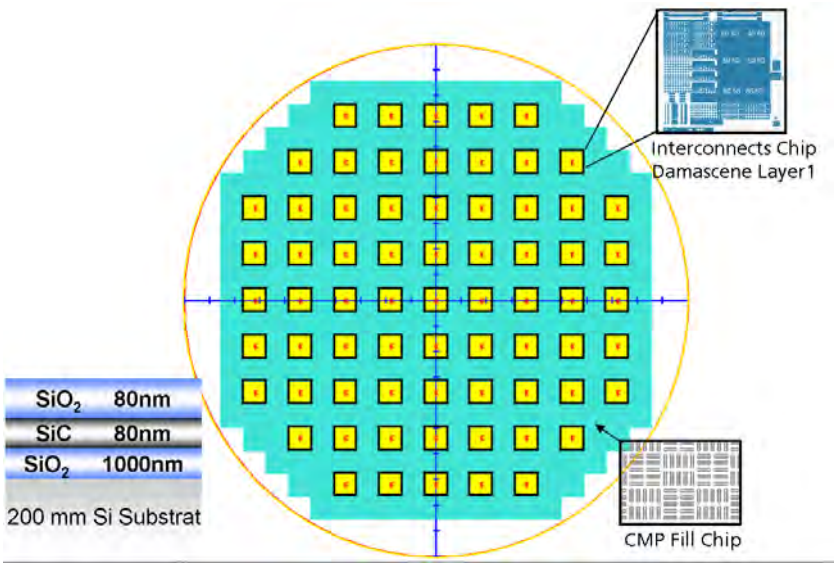
To realize fast and efficient Integrated Circuits the interconnect system gains an increasing importance.
In particular, this is the case for logic and processor circuits with up to 10 metallization layers.
For the optimization of this technology and individual processes it is desirable to flexibly produce test structures with a small lot number. In contrast to standard optical lithography using masks electron beam lithography can deliver such test chips in a flexible, fast and inexpensive way. Furthermore, critical dimensions of future technology nodes can be produced which are not yet manufacturable by standard optical lithography tools.
For demonstrating the potential of modern E-Beam Direct Write (EBDW) systems for this application Copper damascene interconnect lines in dielectrics with critical dimension down to 50nm have been produced. In this joined Fraunhofer collaboration the blank wafers were delivered by Fraunhofer ENAS and exposed using the state-of-the-art variable-shaped E-Beam system at Fraunhofer CNT. Fraunhofer ENAS again successfully developed the following processes to transfer the produced resist pattern into the wafer stack. Based on the collaboration between CNT and ENAS in 2010, it is planned to proceed with the next process steps: after chemical-mechanical polishing (CMP) and applying a SiC capping layer the second E-Beam layer will be patterned. This layer will define the etching window for the subsequent Air-Gap formation. The produced interconnect test pattern will be electrically analyzed to measure the resistance-capacitance product.

Summary of E-Beam Litho at Fraunhofer CNT for interconnect lines:

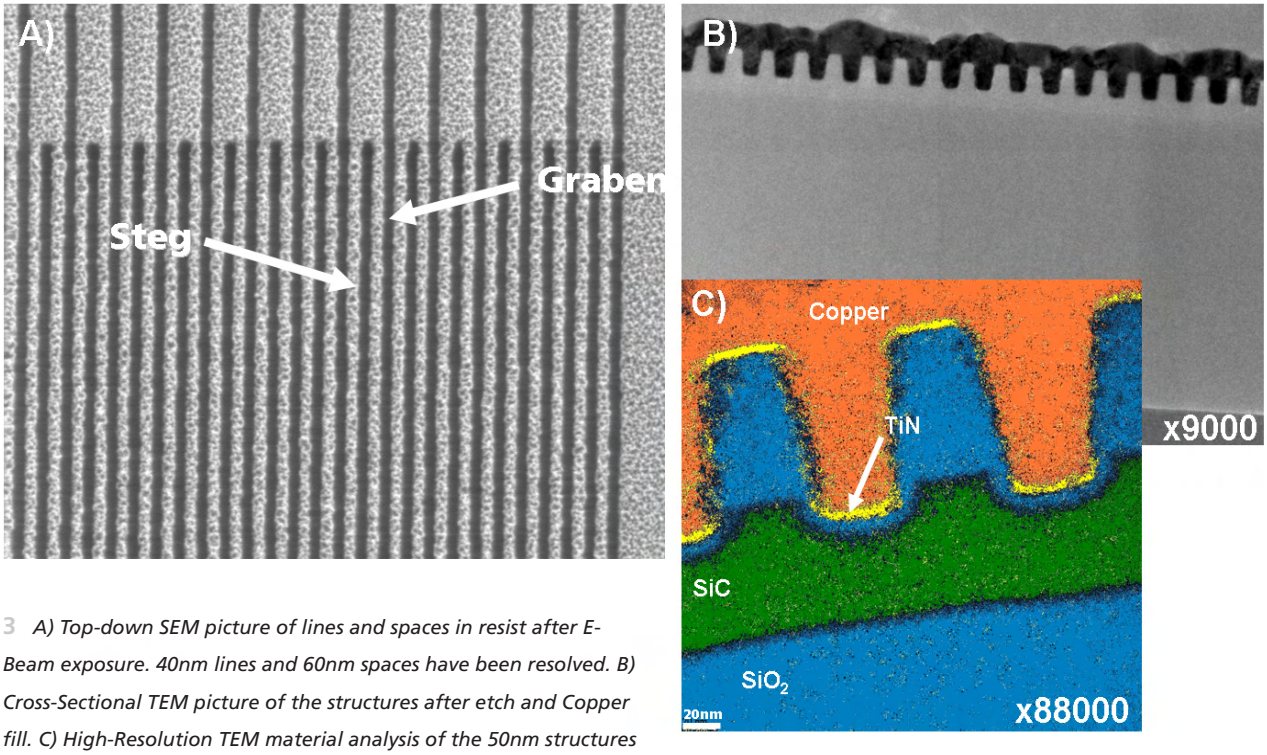
- Pattern: Low-k / Cu - Damascene structures and CMP filling structures (Dummy Patterns)
- Critical dimensions (lines and spaces): 50 nm – 200 nm
- Types of structures: dense lines, isolated lines, Vias (contact holes)
- Stack: SiO_2 on SiC
- Resist: thickness 80 nm, tonality positive, chemically amplified



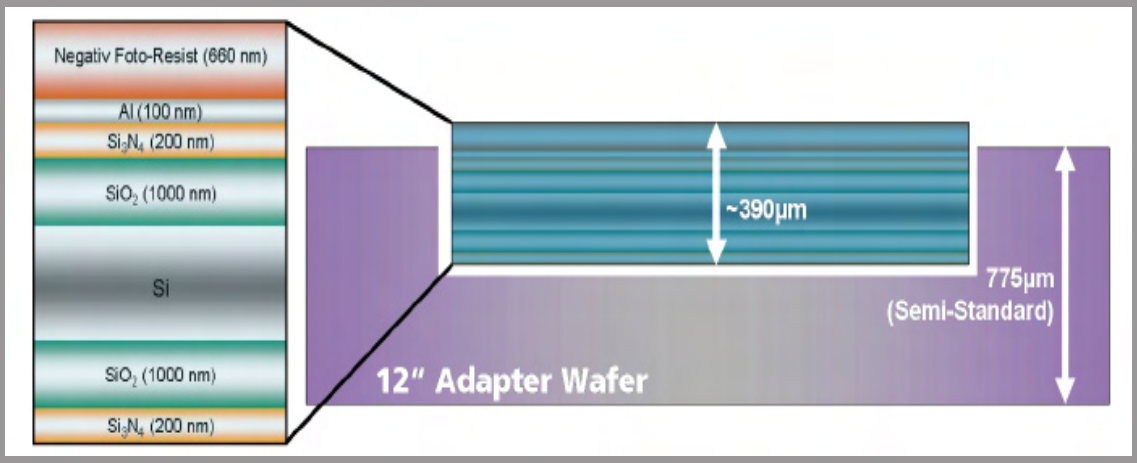
1 *InterConnect lines with Air Gap structure [Source: Fraunhofer ENAS])*



2 *Utilized stack and map of the exposed 200mm wafers.*



3 *A) Top-down SEM picture of lines and spaces in resist after E-Beam exposure. 40nm lines and 60nm spaces have been resolved. B) Cross-Sectional TEM picture of the structures after etch and Copper fill. C) High-Resolution TEM material analysis of the 50nm structures using electron energy loss spectroscopy (EELS).*



4 *For exposing the 400µm thin 8 inch wafers pocket wafer technology has been applied. On the left the utilized wafer stack can be seen..*

MEMS/NEMS E-Beam patterning of a novel Fabry-Pérot-Interferometer

New opportunities in the field of MEMS/NEMS development by using modern E-Beam Lithography have been created. This was successfully demonstrated for Fabry-Pérot-interferometer device product by patterning aluminum ring resonator structures with critical dimensions down to 100nm. This interferometer can for instance be used in future as high-resolution infrared spectrometers.

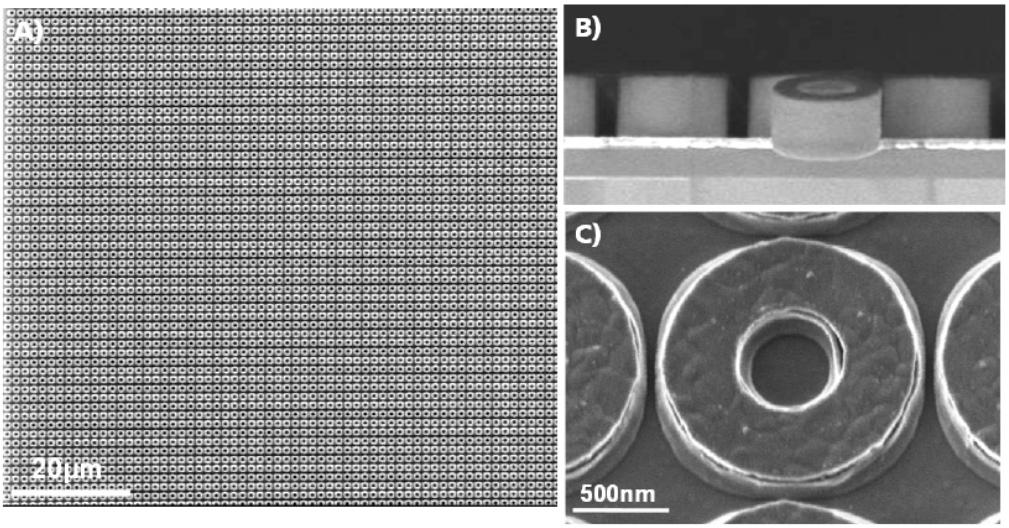
For transfering the resist pattern into the wafer stack new hardmask and etching processes have been developed because standard processes were not suitable for these nanostructures. E-Beam Lithography made it possible to investigate different optical designs of the ring resonator arrays on the wafers. A detailed characterization of the optical functionality will be carried out in follow-up projects in 2010.

For the next steps it steps it is planned to structure the wafers on the back side and bond two wafers together to build a working device which can be optically characterized.
(Dr. Philipp Jaschinsky)

Summary of the E-Beam Litho at Fraunhofer CNT for MEMS/NEMS:

- Pattern: arrays of ring structures with diffrent size and shape
- Critical dimensions: 100 nm to 650 nm
- Stack: 100 nm Aluminium / Si_3N_4 / SiO_2
- Resist: thickness ~600 nm, tonality negative, chemically amplified

5 *A) SEM picture detail of an 800µmx800µm ring array after Aluminum etch step. B.) X-Section picture of resist structures after E-Beam Litho step. C) SEM picture of the aluminum rings after etching and stripping of the resist mask.*



PATTERNING

Resolution limits in electron beam lithography

The target of the research activities, which were performed within the project S0HAR and the European joint project MAGIC, was to achieve a better resolution as well as an improved technological understanding for the use in subsequent projects.
Within the framework of a doctoral thesis the following assumption was verified: For optimized resist processes, the resolution of a state-of-the-art Variable-Shaped-Beam (VSB) writer is comparable with that of a Gaussian-Beam writer. To have a quantitative parameter in addition to the simple determination of the structure width by means of a scanning electron microscope, the total blur was introduced. It combines the resolution limiting error sources like coulomb interactions (beam blur), resist process (process blur) and proximity effect (scattering blur). The total blur shall result from the square root of the squared sums of the mentioned single components. Thereby, the approach was followed in which the influences can be separated by an experimental cross-comparison of the exposure concepts Gaussian-Beam and Variable-Shaped-Beam using chemically amplified and non-chemically amplified resist systems. The experiments were performed under controlled process conditions in the cleanrooms of the Fraunhofer CNT and the French research institute CEA LETI. So the systematical comparison of electron beam writers with different exposure concepts was possible for the first time.
For the comparison, well-defined processes have been developed and were fully characterized. Thereby, a chemically amplified and a non-chemically amplified resist have been chosen and the favored process windows were adjusted.

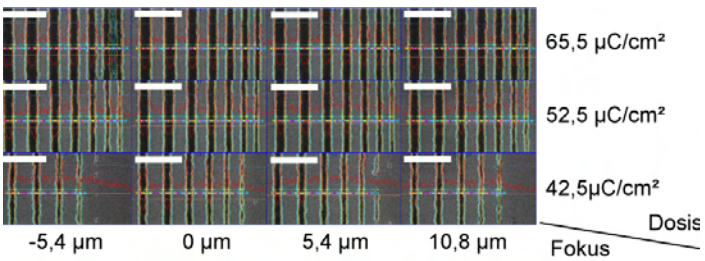
On three representatives out of a series of chemically amplified negative resists (nCARx) investigations were performed regarding the film thickness and its uniformity, the parameters contrast, sensitivity, clearing dose and dark erosion, the influence of the developer, the bake sensitivities after coating and after exposure as well as the achievable resolution. By process optimization a standard process with a good contrast value, a maximized process latitude and a low threshold dose was defined. Furthermore, the resist nCAR3 was chosen from the polyhydroxystyrene-based resist series, since it has the best contrast and the lowest bake sensitivity. Its relaxed aspect ratio due to the smaller film thickness assures a higher resolution, since the collapsing of lines will happen at even smaller line widths.
As non-chemically amplified resist the silicon-containing Hydrogen-Silsesquioxane (HSQ) was chosen. The understanding of this special resist system was boosted by means of the performed process optimization. The required dose for cross-linking strongly depends on the processing. By optimization of the developer attack the contrast of HSQ was improved. Nevertheless, when using the CMOS-compatible developer TMAH with a concentration of 2,38%, the contrast is almost one order of magnitude smaller than for nCAR3. By variation of the film thickness its significant influence on contrast and basedose was shown. Furthermore, HSQ was processed on 300 mm wafers for the first time. Due to the small volumes the resist was dosed with a small volume dispense unit.

PATTERNING

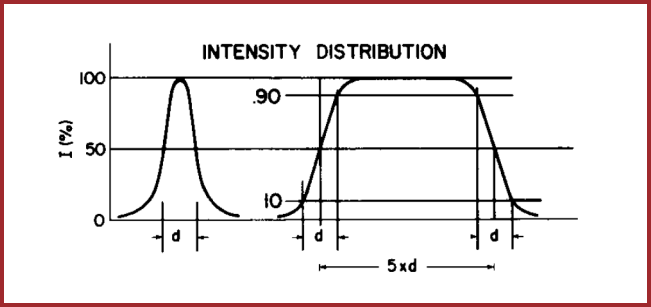
For the experimental cross-comparison conventional methods were successfully adapted or new interpreted for electron beam lithography and new approaches were introduced. The contrast of a resist is an important instrument for the process characterization. Via ellipsometrical measurement of the contrast curve and the subsequent calculation of the contrast using a Lorentz fit of the first derivative of the normalized film thickness, the resist contrast can be determined in an objective and repeatable way. Then it can be used for process characterization and control. Furthermore, every exposure needs a defined working point in dependency on resist thickness, substrate and layer stack, acceleration voltage, calibration of the electron beam writer as well as the used resist. For its determination the so called basedose was defined and successfully linked with the contrast curve. With the help of the parameters contrast, basedose and process latitude the resist process on 200 mm and 300 mm wafers was compared and fine-tuned for different electron beam writers and acceleration voltages.

The isofocal dose method turned out to be a convenient instrument. It was shown that the isofocal dose (where the structure widths do not depend on the varying focus) is independent of the exposure concept and the beam profile, when the process is kept constant. Furthermore, the method can be used to determine the process window. From the comparison of the electron beam writers it can be deduced that the process window is larger with a higher acceleration voltage. An important result is that VSB writer with the same acceleration voltage are less prone to process fluctuations than Gaussian-Beam writers. Besides the structure width, the isofocal dose method was successfully applied for the analysis of resolution and line width roughness with varying focus.

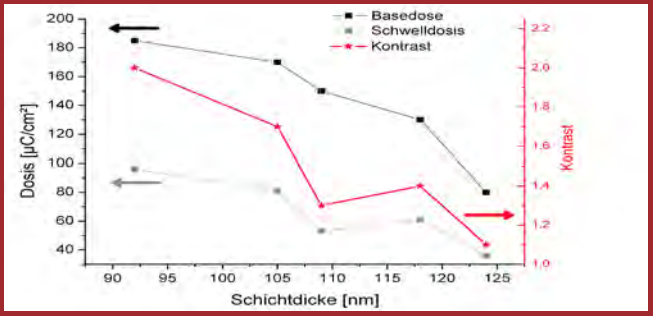
For the determination of the total blur under varying focus, the isofocal dose method was extended with a special spatial frequency modulated pattern. Therewith, the focus dependency of the total blur was demonstrated and quantified. The dependency induces problems for the proximity effect correction.



3 *CD-SEM images of a focus-dose-matrix of the frequency-modulated pattern (resist nCAR3, 50 kV Gaussian-Beam writer, scale bar 200 nm)*



1 *Intensity profile of a Gaussian-Beam writer (left) and a Variable-Shaped-Beam writer (right) [JVSTB 12 (1975) 1170]*



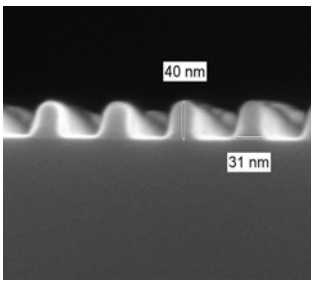
2 *Base dose, threshold dose and contrast of HSQ at different resist film thicknesses*

For both resist systems on VSB and Gaussian-Beam writers, the total blur was determined in the best focus point by means of the mentioned method. With both resist systems the largest values of the total blur (25 nm/ nCAR3, 50 nm/ HSQ) were achieved for the 50 kV VSB writer and the smallest values (17 nm/ nCAR3, 36 nm/ HSQ) for the 100 kV Gaussian-Beam writer. Since the resolution limiting diffusion effect occurs only together with chemically amplified resists, smaller values of the total blur were expected for the non-chemically amplified resists. However, these values are only reachable with CMOS-incompatible developers (TMAH with a concentration of 25% e.g.). Anyhow, the correlation of the total blur and the resolution of dense lines was shown with the aid of the modulation transfer function (which is the Fourier transform of the proximity function and contains the total blur) and the critical modulation transfer function (a modulation of parameters of the contrast curve). Experimentally this was done for both resist systems in combination with the VSB and Gaussian-Beam writers. The best resolution of dense lines with 31 nm was shown by the 50 kV VSB writer, this value is identical with the independently determined intersection point of the modulation transfer function and the critical modulation transfer function. The resolution of the Gaussian-Beam writers for the exposure of the chemically amplified resist was worse (36 nm/ 100 kV) due to the higher current density. In the non-chemically amplified resist the best resolution of dense lines with 36 nm was also shown by the 50 kV VSB writer.

With a smaller total blur the resolution of dense lines is improved. However, this is not completely valid for VSB writers due to their format change (and refocusing) in dependency on the line width. Since the current density is constant, the beam current drops proportional with the area of the shot, which causes the reduction of the beam blur and hence of the total blur. Since high resolution was not needed for the determination of the total blur, the test pattern was exposed with larger shots and consequently induces a larger total blur.

Concerning the single components of the total blur, several conclusions can be drawn. The scattering blur, which means the forward scattering, is irrelevant using resist thicknesses smaller than 100 nm and acceleration voltages of 50 kV or larger. The process blur makes the largest fraction of the total blur. Furthermore, the beam blur of the VSB writer is variable: In dependency on the shot size a process-dependent regime or a column-dependent regime exists.

(Katja Keil)



4 *Resolution of dense lines in cross-section (resist nCAR3, 50 kV VSB writer)*

PUBLICATIONS

Research and Development at highest technological level requires intensive information networking with potential cooperation partners and customers. At numerous events such as colloquia and workshops Fraunhofer CNT presented its innovative services and application solutions for industry and society.

„Lange Nacht der Wissenschaften"

Six Fraunhofer Institutes presented their impressing attractions at the „7. Langen Nacht der Wissenschaften" on July 19, 2009. The Fraunhofer CNT took its visitors on a journey into the world of nano-electronics - beamed within smallest dimensions. The institute presented its research activities „on the edge of imagination" with the help of the model „From sand to superchip". Using that model the history of the development of a computer chip can be explained very understandable. Furthermore, Fraunhofer CNT and its visitors examined wafer pieces and offered a talk with the topic „Erweiterung der Sinne: Analytik zur Nanoelektronik" to all sly dogs, junior scientists and all interested visitors.

Tutorial

On May 13/14, 2009 Prof. Ernest Levine gave his lecture on „Integrated Ciruit Fabrication & Yield Control" at Fraunhofer CNT. Prof. Ernest Levine's specialty is chip fabrication. A faculty member at College of Nanoscale Science and Engineering of the University of Albany, USA - the most advanced research complex of its kind at any university in the world – Levine draws upon his 25 years of experience at IBM working on diverse problems associated with building devices and interconnects. His liverly engaging style is toprated by past course attendees. Students were able to learn the basics of chip fabrication from an expert - from basic transistors to step-by-step build sequences including the latest on 45 nm node and below.

SEMICON Europe 2009

On October 8, 2009 SEMICON Europe closed in Dresden. For the first time the leading trade show for the european semiconductor industry took place at the Capital of Saxony. Among 400 exhibitors Fraunhofer CNT joint the booth of Fraunhofer Group for Mircoelectronics. The Fraunhofer CNT presented its latest technologies as well as its innovative research results.

International Visits

Organized by the Ministry of Foreign Affairs a group of international journalists visited our institute in order to talk about the „Investment location Germany" on June 18, 2009. Dr. Knut Nevermann, State Secretary at SMWK and Prof. Dr. Peter Kücher, director of Fraunhofer CNT, discussed together with the journalists topics such as „Innovation, Technology and Fields of Excellence in Saxony". The visitors also joint a guided tour alongside the institut's lab and clean-room facilities. Therefore, the delegation gained an interesting insight into the diverse R&D activities of Fraunhofer CNT.

Colloquia

"Epitaxial Lanthanide Oxide for Si-based Electronics"
Dr. H. J. Osten - Institute of Electronic Materials and Devices, Leibniz University Hannover

"Analytische Methoden für die Untersuchung der Synthese geträgerter Edelmetallpartikel und komplexer Mischoxide"
Dr. Jörg Radnik – Leibniz-Institute of für catalysis, University Rostock/Berlin

"Formation and Characterization of Si/Ge Nanostructures at the Atomic Level"
Bert Voigtländer - Institute of Bio- and Nanosystems, and JARA-Fundamentals of Future Information Technology, Forschungszentrum Jülich

"Controlling Photons Using Semiconductor Nanostructures"
Dr. Mohamed Benyoucef - Institute for Integrative Nanosciences, IFW Dresden

"Transmission electron microscopic analysis of vapour-liquid-solid grown semiconductor nanowires"
Dr. Holm Kirmse - Humboldt-Universität Berlin, Institute of Physics, AG Crystallography

„Development of GeSbTe Films by Atomic Vapor Deposition for Phase Change Memory Applications"
Prof. Michael Heuken – VP Corporate Research & Development, AIXTRON AG

„Si-Dünnschicht Solartechnologie: Glasbeschichtung oder Mikroelektronik auf großen Substraten?"
Dr. K.-H. Stegemann – VP Technology Signet Solar GmbH

„Industrial Applications of Atomic Layer Deposition Including Thin Film Materials for PV and SOFC Applications"
Prof. Lauri Niinistö - Helsinki University of Technology

2. Colloquium CMOS Technology / Microelectronic „Physical Analytics" June 23, 2009

Presentation of Infineon Technologies Dresden GmbH:
„Allgemeine Vorstellung der PFA bei Infineon"
„Globale Fehlerlokalisierung"
„Nanoprobing-Center"

Fraunhofer CNT:
„Materialanalyse mit Ionen und Röntgenstrahlen"

PUBLICATIONS

Besides R&D activities publishing the gained results within a scientific article or at a scientific journal is an important part of every research performance.

Best Scientific Paper Award

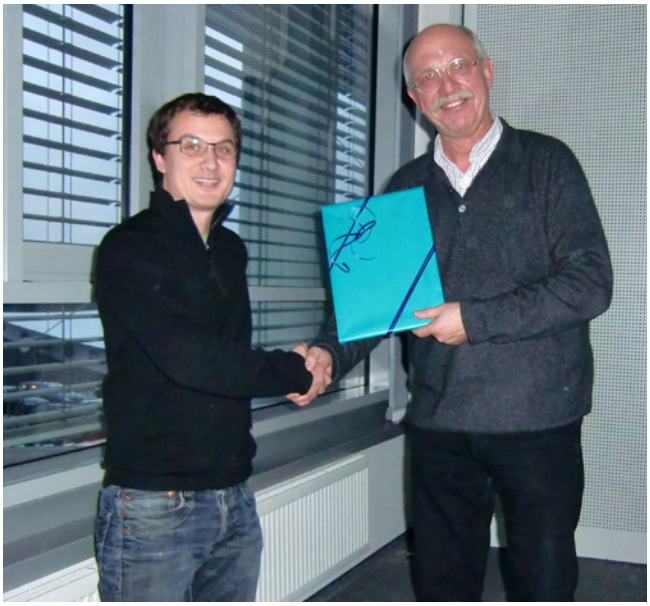
The „Best Scientific Paper Award 2009" received our Ph.D. Student Thomas Oszinda for his scientific contributions to the following conferences:

„Chemical Repair of plasma damaged porous ultra low-k SiOCH film using different chemicals"
ECS (Electrochemical Society Conference), 13.-15.10.2009, Vienna, Austria

„Restoration of plasma damaged porous SiOCH: A coating process with UV activation versus a vapor phase process with thermal activation"
AMC (Advanced Metalization Conference), 4.-9.10.2009, Baltimore, USA

„Characterization of plasma damaged porous ULK SiCOH layers in aspect of changes in the diffusion behavior of solvents and repair chemicals"
IEEE 2009 (International Interconnect Technologie Conference), 1.-3.06.2009, Sapporo, Japan

„Investigation of physical and chemical properties of ultra low-k SiOCH in aspect of cleaning and chemical repair processes"
MAM 2009 (Materials for Advanced Metallization Conference), 8.-11.03.2009, Grenoble, France



1 *Prof. Peter Kücher hands over the „Best Scientific Paper Award" to Thomas Oszinda, Ph.D. Student at Fraunhofer CNT*

Patents

2009 scientists at Fraunhofer CNT were involved in five invention disclosures. Two of them were applied for a patent. The remaining three were transfered onto the partners, according to contractually agreement.

Two patent applications:

„Verfahren zur Verringerung der Langzeit-Einsatzspannungsverschiebung bei haftstellenbasierten, nichtflüchtigen Speicherzellen“
Raik Hoffmann, Thomas Melde (Uni Freiberg)

„Verfahren zur Bestimmung von Parametern einer Proximity-Funktion, insbesondere für die Korrektur des Proximity-Effektes bei der Elektronenstrahllithografie“
Marc Hauptmann, Katja Keil, Dr. Philipp Jaschinsky, Dr. Kang-Hoon Choi, Manuela Gutsch

Diploma thesis

„Untersuchung und Optimierung der Kostenverrechnung im Fraunhofer CNT“
Kay Deutscher

„Elektrische Charakterisierung von Atomic Layer Deposition high-k Dielektrika in MIM Strukturen“
Dzmitry Dudkevich

Beug, M. F.; Melde, T.; Paul, J.; Bewersdorff-Sarlette, U.; Czernohorsky, M.; Beyer, V.; Hoffmann, R.; Seidel, K.; Löhr, D. A.; Bach, L.; Knoefler, R.; Tilke, A.:
„Improvement of 48 nm TANOS NAND Cell Performance by Introduction of a Removable Encapsulation Liner"
IEEE International Memory Workshop 2009, Monterey, USA; Vol. 10-14, pages: 1 – 2

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„Tailoring the Si_3N_4/Al_2O_3 interface in TANOS non-volatile memory stack fabrication"
40th IEEE Semiconductor Interface Specialists Conference (SISC), 2009, Arlington, USA

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„In-situ ARXPS analysis of ultrathin TaNx barrier films on SiCOH"
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„Utilizing near-field and depolarization effects for tip-enhanced Raman spectroscopy on semiconductor nanostructures"
DPG Frühjahrstagung 2009, Dresden

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The 25th European Mask and Lithography Conference EMLC 2009; Proc. of SPIE Vol. 7470, 747017, Dresden

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„Resolution and Total-Blur: Correlation and Focus Dependencies in E-Beam Lithography"
EIPBN 2009, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 27, issue 6, page 2722

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„Thin ZrO_2 films on 300 mm wafers by Sin-Coating Technique – Processing & Characterisation"
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„Influence of Additive Co-adsorption on Copper Fill Behavior"
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„Analysis of Boron delta layers with LEAP"
Microscopy and Microanalysis 2009, Richmond, USA

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„Atomic scale materials analysis for advanced transistors applying Atom Probe Tomography"
Microscopy and Microanalysis 2009, Richmond, USA

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EDITORIAL NOTES

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