



# MEMS Technologies Dresden

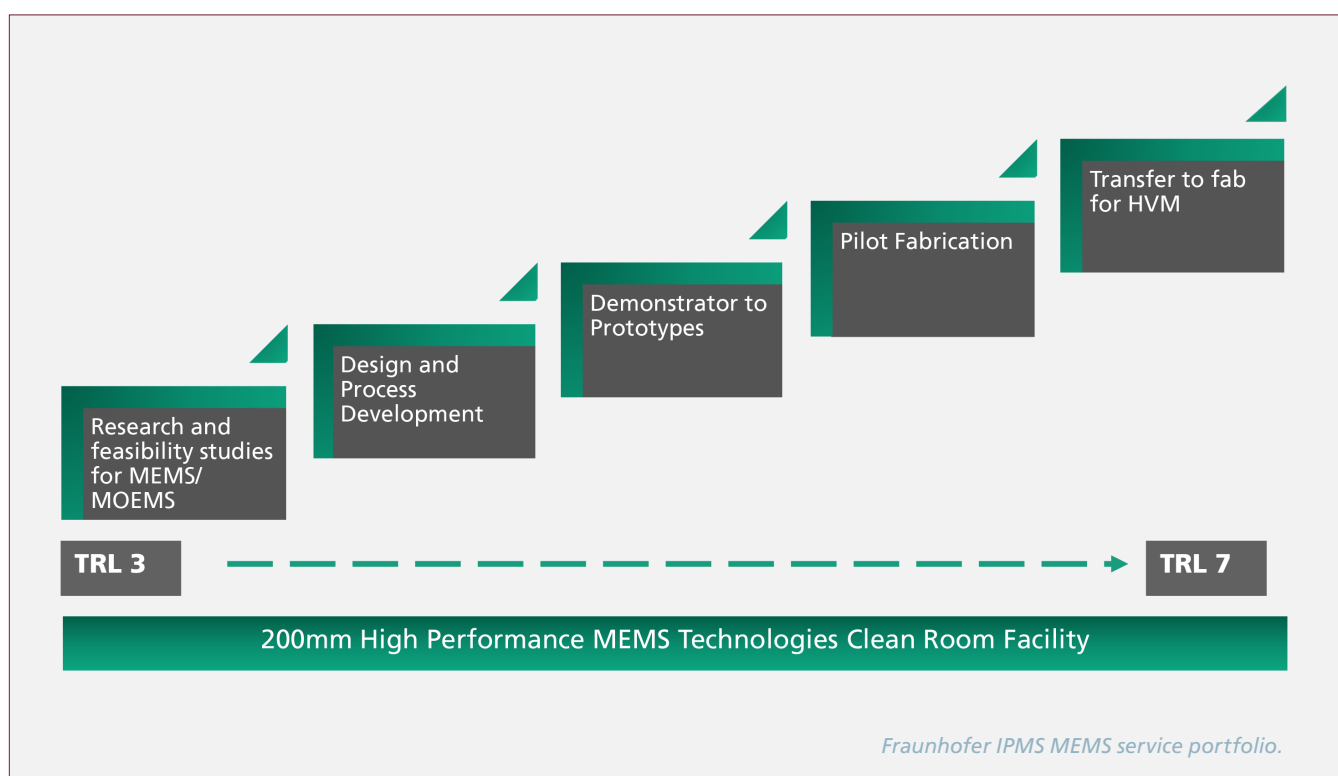
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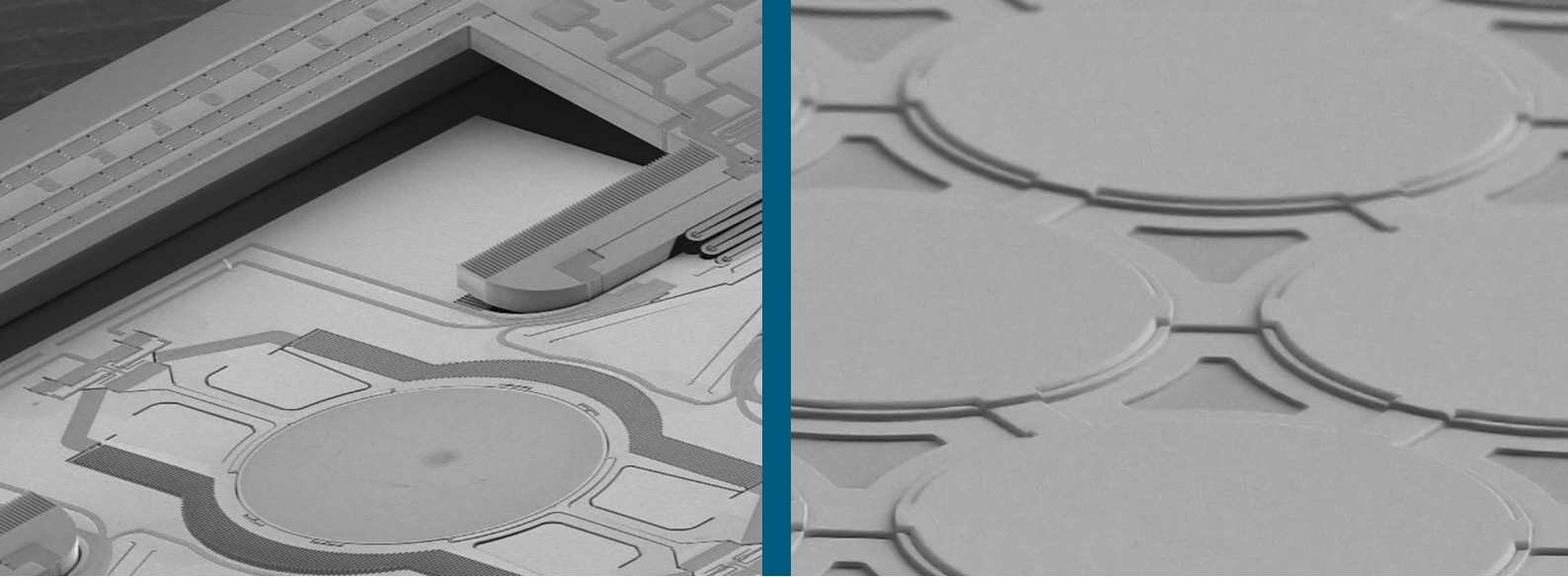




# Services at a Glance

Fraunhofer IPMS develops micro-electro-mechanical (MEMS) and micro-opto-electro-mechanical (MOEMS) systems, products and technologies. Using our 200 mm state-of-the-art clean room facility, our services range from feasibility studies to process technology development all the way to complete fabrication processes including prototyping and pre-series manufacturing for the rapidly growing fields of sensors and actuators. We are offering our deep technological expertise in the fields of bulk MEMS and surface MEMS as well as the monolithic integration of MEMS-on-CMOS.



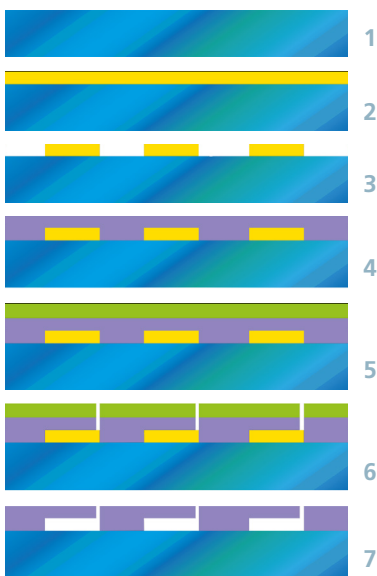


# Manufacturing Technologies

## Surface Micromachining

Fraunhofer IPMS generates surface micromachined microstructures applying sequences of deposition and etching processes of multiple structural layers. Moveable devices such as spatial light modulator or CMUTs are manufactured.

- PE-CVD for sacrificial layers
- Five-zone CMP for high planarity
- Gas phase etch release ( $\text{HF} + \text{XeF}_2$ )
- ALD for barrier layer
- Anti-stiction layer

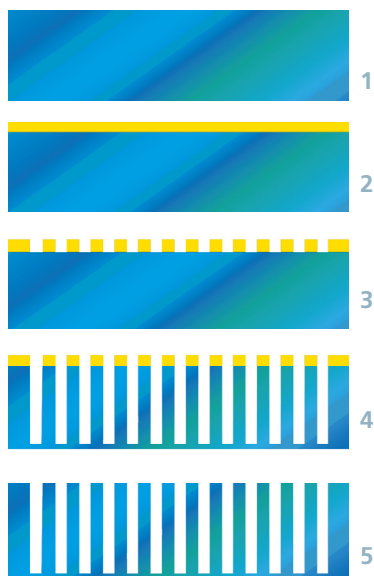


1 bare silicon wafer 2 sacrificial layer  
3 patterning 4 moveable part 5 top mask  
6 patterning & etching 7 GPE release

## Bulk Micromachining

Bulk micromachining allows us to create moveable and electrically isolated three-dimensional structures into silicon substrate (the bulk). Using excellent mechanical and electrical (by doping) properties of monocrystalline silicon.

- DRIE up to AR > 30
- TMAH etch for backside opening
- PVD for high reflectivity coatings
- Grinder for thinning
- Trench filling for isolation



1 bare silicon wafer 2 hard mask 3 hard mask  
patterning 4 DRIE etching 5 mask removal

## Active silicon

Fraunhofer IPMS Dresden manufactures wafer-level devices that utilize the chemical and physical properties of functional layers, for example in the ion-sensitive field-effect transistor for the measurement of pH values.

- Thermal oxidation for gateoxide ( $\text{SiO}_2$ )
- Annealing (RTP/RTA)
- TMAH Etch for backside opening
- Deposition of active layers (e.g.  $\text{Ta}_2\text{O}_5$ )

## MEMS-on-CMOS technology

Fraunhofer IPMS is offering the complete manufacturing chain to apply surface and bulk micromachining on customized CMOS substrates for applications such as spatial light modulators, capacitive micro-machined ultrasonic or actuator arrays. Using foundry-fabricated CMOS backplanes, we are able to shorten development times for these highly integrated devices focusing on MEMS-CMOS interface, MEMS integration and fabrication.



- R&D and pilot fabrication (low volume & high mix)
- 24/5 – 3 shift operations
- Class 10 (ISO 4) on 1.500 m<sup>2</sup>
- ISO 9001:2015 certification
- 45 engineers + 45 operators and maintenance techs running the cleanroom
- 365 nm i-line (400 nm I&S)
- 248 nm DUV (130 nm I&S)
- ~1.000 wafer starts per month
- CMOS compatible
- MES for planning, traceability and documentation

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